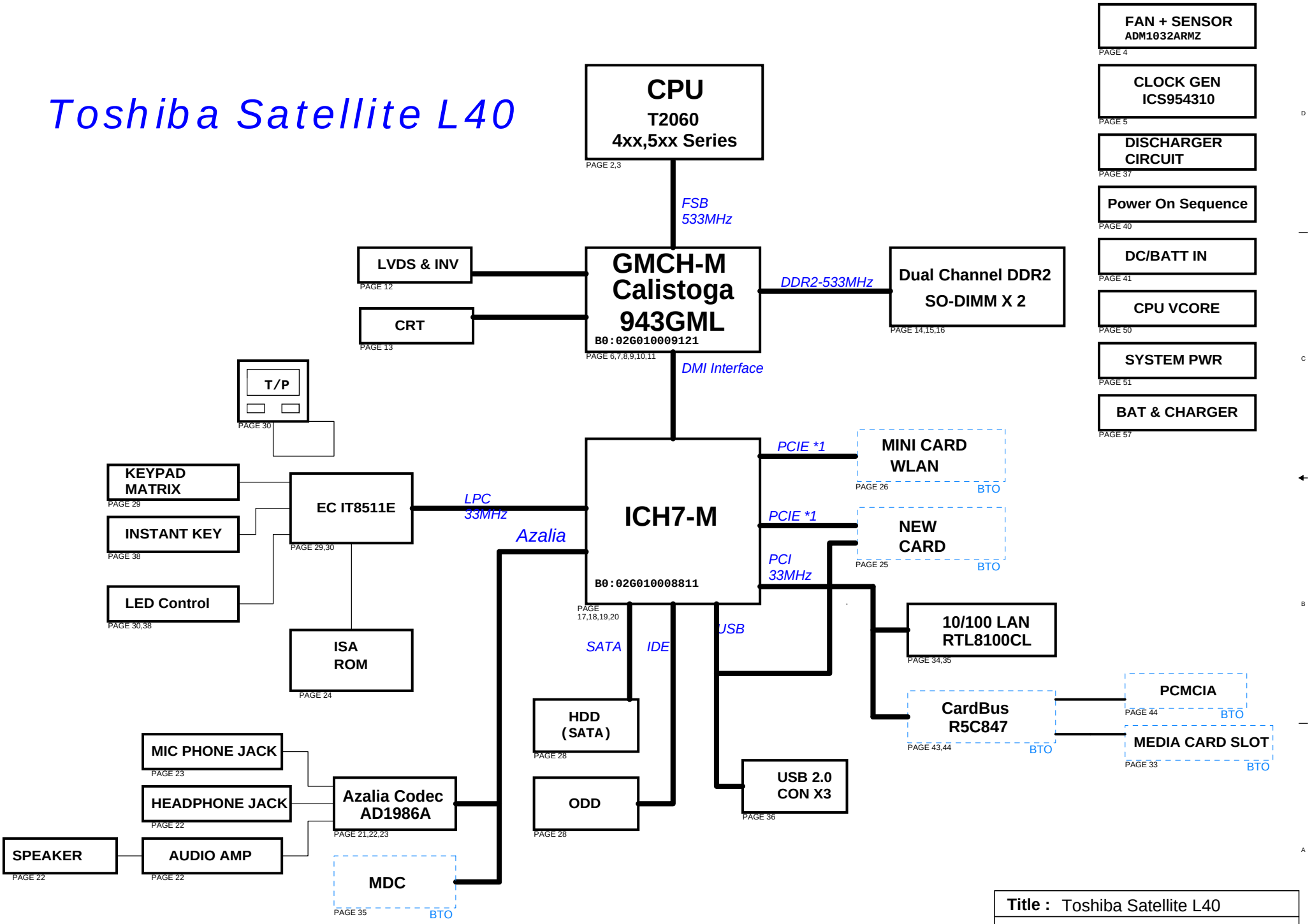
Toshiba Satellite L40



Title :	Toshiba Satellite L40	
Size	Project Name: Toshiba Satellite L40	Rev: 1.1
Date:	Sheet of	

6 H_A#[16..3]
6 H_REQ#[4..0]
6 H_A#[31..17]

U201A

ADDR GROUP 0
A[3]# J4
A[4]# L4
A[5]# M3
A[6]# K5
A[7]# M1
A[8]# N2
A[9]# J1
A[10]# N3
A[11]# P5
A[12]# P2
A[13]# L1
A[14]# P4
A[15]# P1
A[16]# R1
ADSTB[0]# L2
REQ[0]# K3
REQ[1]# H2
REQ[2]# K2
REQ[3]# J3
REQ[4]# L5

ADDR GROUP 1
A[17]# Y2
A[18]# U5
A[19]# R3
A[20]# W6
A[21]# U4
A[22]# Y5
A[23]# U2
A[24]# R4
A[25]# T5
A[26]# T3
A[27]# W3
A[28]# W5
A[29]# Y4
A[30]# W2
A[31]# Y1
ADSTB[1]# V4

THERM
A20M# A6
FERR# A5
IGNNE# C4

HCLK
STPCLK# D5
LINT0 C6
LINT1 B4
SMI# A3

RESERVED
RSVD[1] AA1
RSVD[2] AA4
RSVD[3] AB2
RSVD[4] AA3
RSVD[5] M4
RSVD[6] N5
RSVD[7] T2
RSVD[8] V3
RSVD[9] B2
RSVD[10] C3
RSVD[11] B25
RSVD[12] T22
RSVD[A2] A2
RSVD[13] D2
RSVD[14] F6
RSVD[15] D3
RSVD[16] C1
RSVD[17] AF1
RSVD[18] D22
RSVD[19] C23
RSVD[20] C24

CONTROL
ADS# H1
BNR# E2
BPRI# G5
DEFER# H5
DRDY# F21
DBSY# E1
BR0# F1
IERR# D20
INIT# B3
LOCK# H4
RESET# B1
RS[0]# F3
RS[1]# F4
RS[2]# G3
TRDY# G2
HIT# G6
HITM# E4

XDP/ITP SIGNALS
BPM[0]# AD4
BPM[1]# AD3
BPM[2]# AD1
BPM[3]# AC4
PRDY# AC2
PREQ# AC1
TCK AC5
TDI AA6
TDO AB3
TMS AB5
TRST# AB6
DBR# C20

PROCHOT# D21
THERMDA A24
THERMDC A25
THERMTRIP# C7

BCLK[0] A22
BCLK[1] A21

H_ADS# H_ADS# 6
H_BNR# H_BNR# 6
H_BPRI# H_BPRI# 6
H_DEFER# H_DEFER# 6
H_DRDY# H_DRDY# 6
H_DBSY# H_DBSY# 6
H_BR0# H_BR0# 6
H_IERR#
H_INIT# H_INIT# 17
H_LOCK# H_LOCK# 6
H_CPURST# H_CPURST# 6
H_RS#0 H_RS#0 6
H_RS#1 H_RS#1 6
H_RS#2 H_RS#2 6
H_TRDY# H_TRDY# 6
H_HIT# H_HIT# 6
H_HITM# H_HITM# 6

H_ADSTB#0 6
H_ADSTB#1 6
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4

H_A20M# 17
H_FERR# 17
H_IGNNE# 17
H_STPCLK# 17
H_INTR 17
H_NMI 17
H_SMI# 17

CPU_THRM_DA 4
CPU_THRM_DC 4
PM_THRMTRIP# 4,17
CLK_CPU_BCLK 5
CLK_CPU_BCLK# 5

T202
R201 56Ohm
+VCCP_AGTL+
R202 54.9Ohm @
T201
R203 R204 R205 R206 R207 R208 56Ohm
R203 56Ohm@
R206 56Ohm@
T203
T204 TPC28T
GND

(070122)Change CPU Socket into PN=12G011204796

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

JP201 @
+VCCP_AGTL+ +VCCP
SHORT_PIN
2.5A
+VCCP 6,9,20,52
+VCCP_AGTL+ 3,5,6,9

29 H_PROCHOT_S#
H_PROCHOT_S# 1
R217 56Ohm
R218 56Ohm@
H_PWRGD 1

H_D#[0..63] 6

U201B

DATA GRP 0
H_D#0 E22
H_D#1 E24
H_D#2 E26
H_D#3 H22
H_D#4 E23
H_D#5 G25
H_D#6 E25
H_D#7 E23
H_D#8 K24
H_D#9 G24
H_D#10 J24
H_D#11 J23
H_D#12 H26
H_D#13 F26
H_D#14 K22
H_D#15 H25
H_DSTBN#0 H23
H_DSTBP#0 G22
H_DINV#0 J26

DATA GRP 1
H_D#16 N22
H_D#17 K25
H_D#18 P26
H_D#19 R23
H_D#20 L25
H_D#21 L22
H_D#22 L23
H_D#23 M23
H_D#24 P25
H_D#25 P22
H_D#26 P23
H_D#27 T24
H_D#28 R24
H_D#29 L26
H_D#30 T25
H_D#31 N24
H_DSTBN#1 M24
H_DSTBP#1 N25
H_DINV#1 M26

DATA GRP 2
D[32]# AA23 H_D#32
D[33]# AB24 H_D#33
D[34]# Y24 H_D#34
D[35]# V26 H_D#35
D[36]# W25 H_D#36
D[37]# U23 H_D#37
D[38]# U25 H_D#38
D[39]# U22 H_D#39
D[40]# AB25 H_D#40
D[41]# W22 H_D#41
D[42]# Y23 H_D#42
D[43]# AA26 H_D#43
D[44]# Y26 H_D#44
D[45]# Y22 H_D#45
D[46]# AC26 H_D#46
D[47]# AA24 H_D#47
DSTBN[2]# W24 H_DSTBN#2
DSTBP[2]# Y25 H_DSTBP#2
DINV[2]# V23 H_DINV#2

DATA GRP 3
D[48]# AC22 H_D#48
D[49]# AC23 H_D#49
D[50]# AB22 H_D#50
D[51]# AA21 H_D#51
D[52]# AB21 H_D#52
D[53]# AC25 H_D#53
D[54]# AD20 H_D#54
D[55]# AE22 H_D#55
D[56]# AF23 H_D#56
D[57]# AD24 H_D#57
D[58]# AE21 H_D#58
D[59]# AD21 H_D#59
D[60]# AE25 H_D#60
D[61]# AF25 H_D#61
D[62]# AF22 H_D#62
D[63]# AF26 H_D#63
DSTBN[3]# AD23 H_DSTBN#3
DSTBP[3]# AE24 H_DSTBP#3
DINV[3]# AC20 H_DINV#3

MISC
GTLREF AD26
TEST1 C26
TEST2 D25
BSEL[0] B22
BSEL[1] B23
BSEL[2] C21
COMP[0] R26
COMP[1] U26
COMP[2] U1
COMP[3] V1
DPRSTP# E5
DPSLP# B5
DPWR# D24
PWRGOOD D6
SLP# D7
PSI# AE6

H_DSTBN#0 6
H_DSTBP#0 6
H_DINV#0 6
H_DSTBN#1 6
H_DSTBP#1 6
H_DINV#1 6
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#2 6
H_DSTBN#3 6
H_DSTBP#3 6
H_DINV#3 6

GTL_REF
R209 1KOhm 1%
<500 mil (55 Ohm)
T/B trace 5
Space 25
R213 2KOhm 1%
C201 0.1UF/10V @
@R214 1KOhm
R216 51Ohm
GND

CPU_BSEL0 5
CPU_BSEL1 5
CPU_BSEL2 5

For Celeron M

BCLK	FSB	BSEL2	BSEL1	BSEL0
133MHz	533MHz	L	L	H

(070122)Change CPU Socket into PN=12G011204796

H_COMP0 R210 27.4Ohm 1%
H_COMP1 R211 54.9Ohm 1%
H_COMP2 R212 27.4Ohm 1%
H_COMP3 R215 54.9Ohm 1%

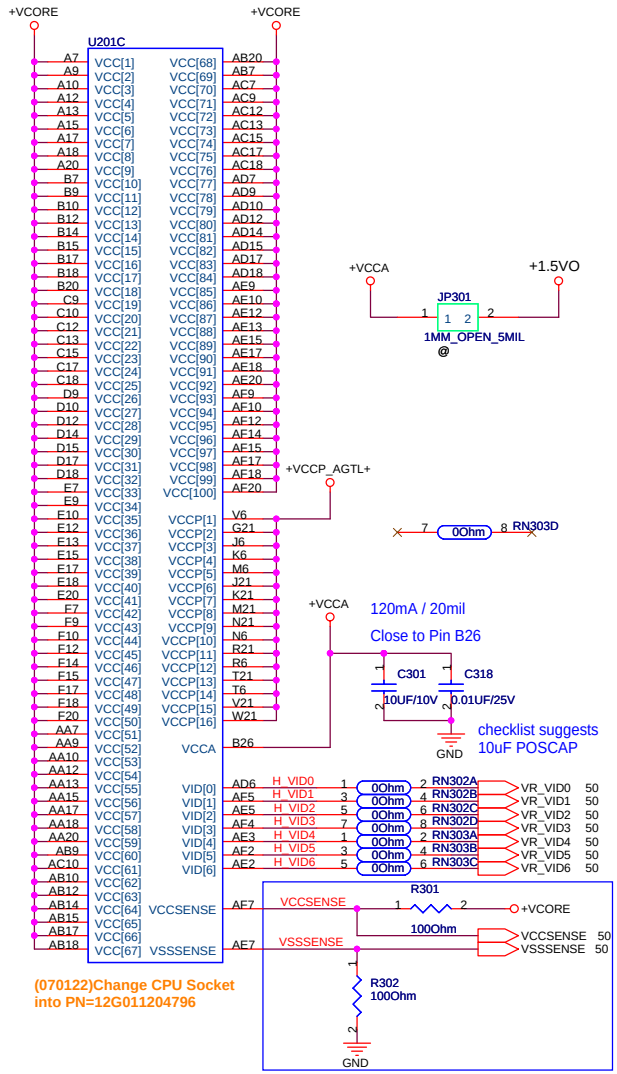
H_DPRSTP# H_DPRSTP# 17,50
H_DPSLP# H_DPSLP# 17
H_DPWR# H_DPWR# 6
H_PWRGD H_PWRGD 17
T205
H_CPUSLP# H_CPUSLP# 6,17
PM_PSI# PM_PSI# 50

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCC	1.0V	1.2V	1.3V
	C3	C2	C0
ICC	14.7A	16.5A	29Ah

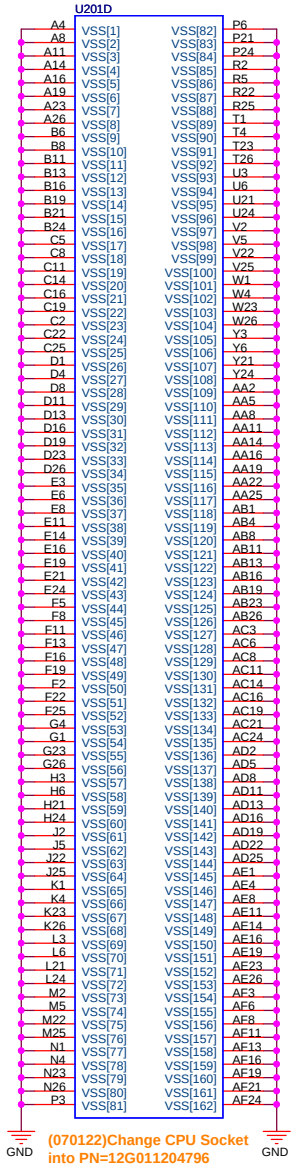
Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
	MIN	TYP	MAX
ICCP			2.5A

Modity Table for Celeron M

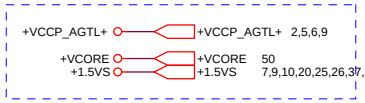


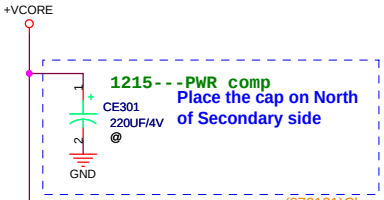
(070122)Change CPU Socket into PN=12G011204796

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.



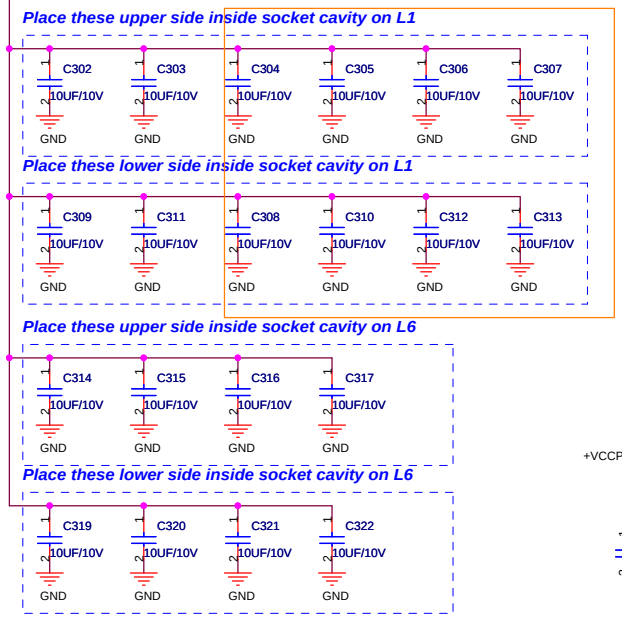
(070122)Change CPU Socket into PN=12G011204796



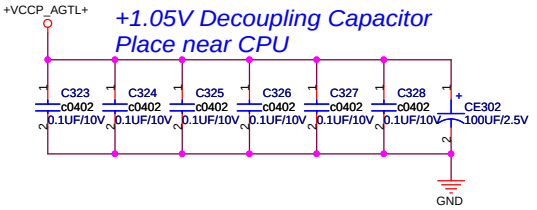


Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

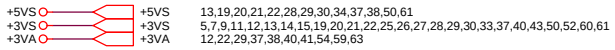
(070131)Change 22UF into 10UF



(061228)Change into 10UF/10V PN:11G236322636360
C302,C303,C309,C311
C314,C315,C316,C317
C319,C320,C321,C322

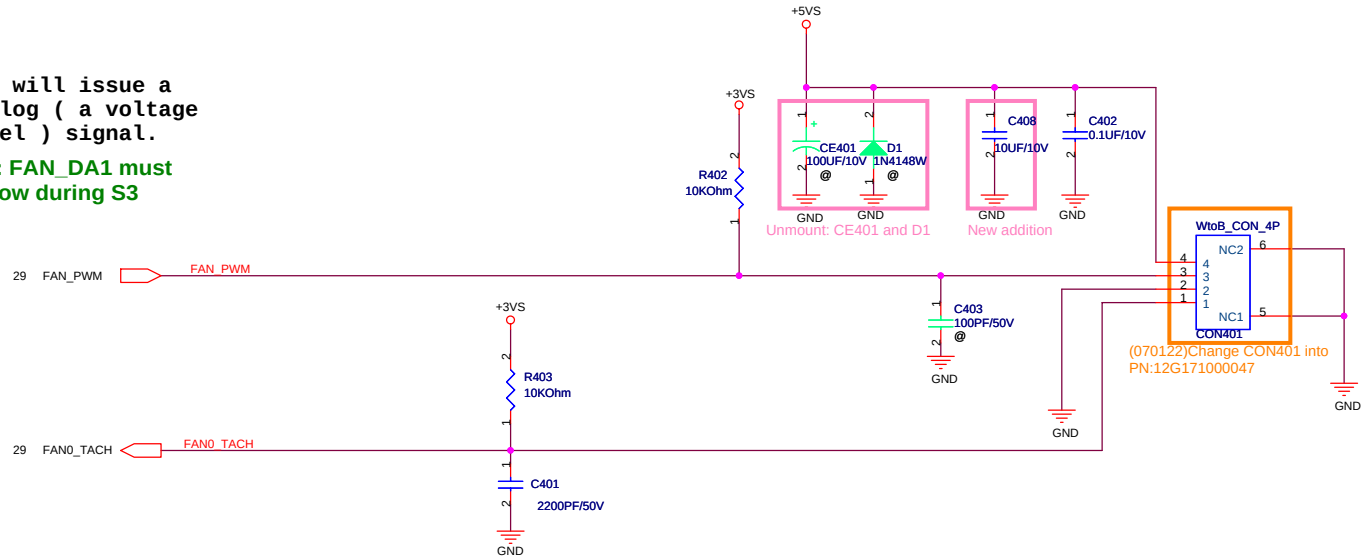


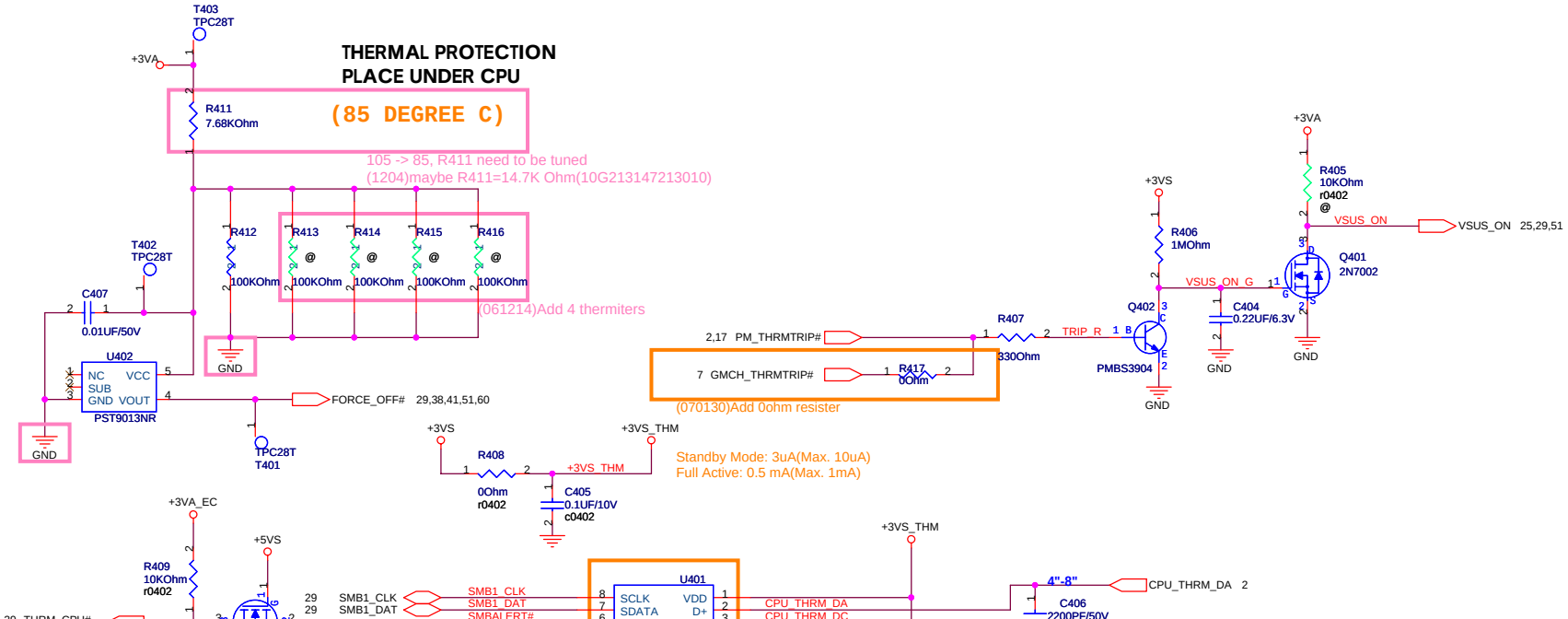
Fan Speed Control



KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

(070130)Change C516 from 27PF to 33PF

Delete CLK_ITPMPCI(connect to pin5)

internal pull high

Remove 0ohm

Realtek:Mount R519,Remove R550 R534

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

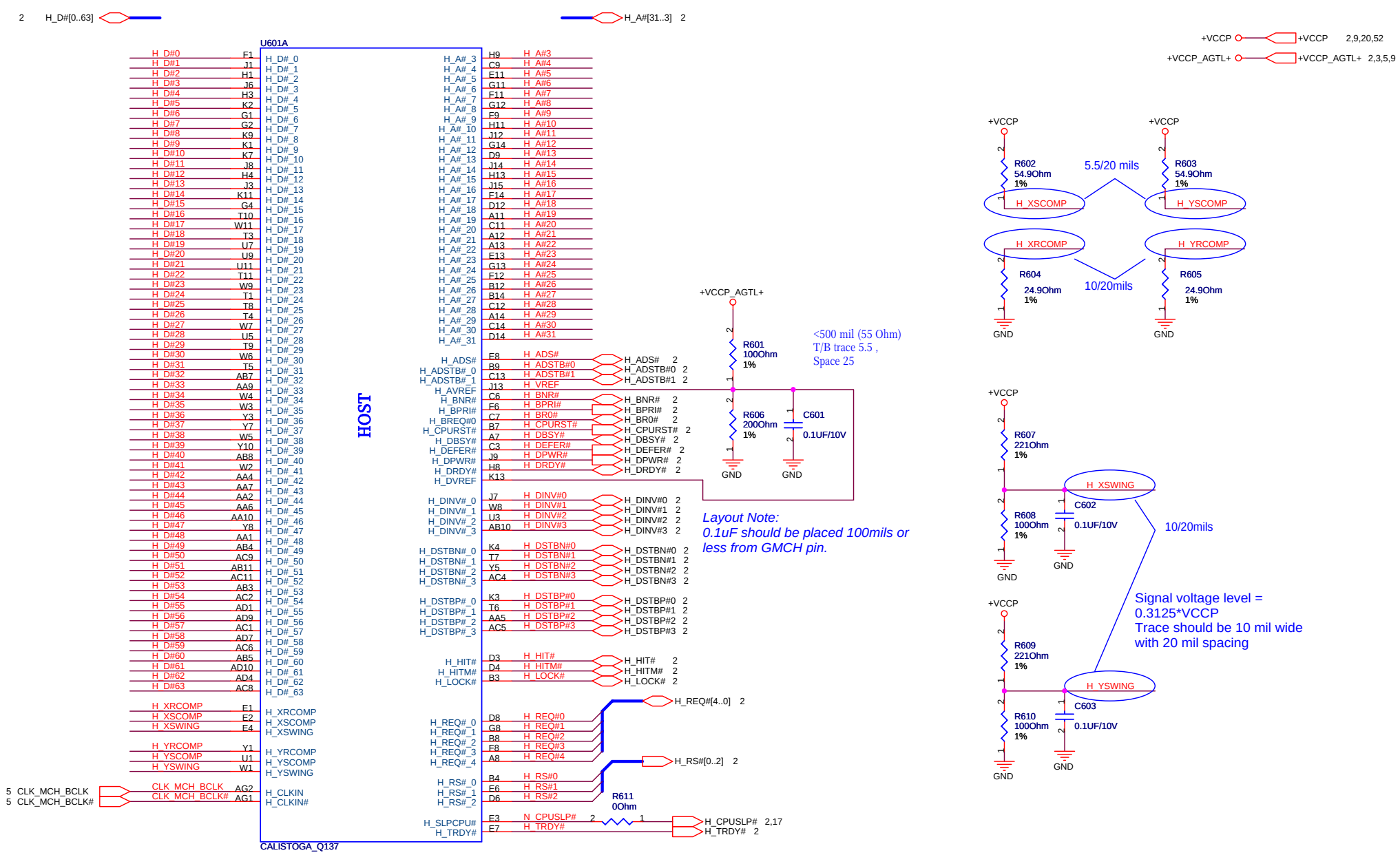
PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

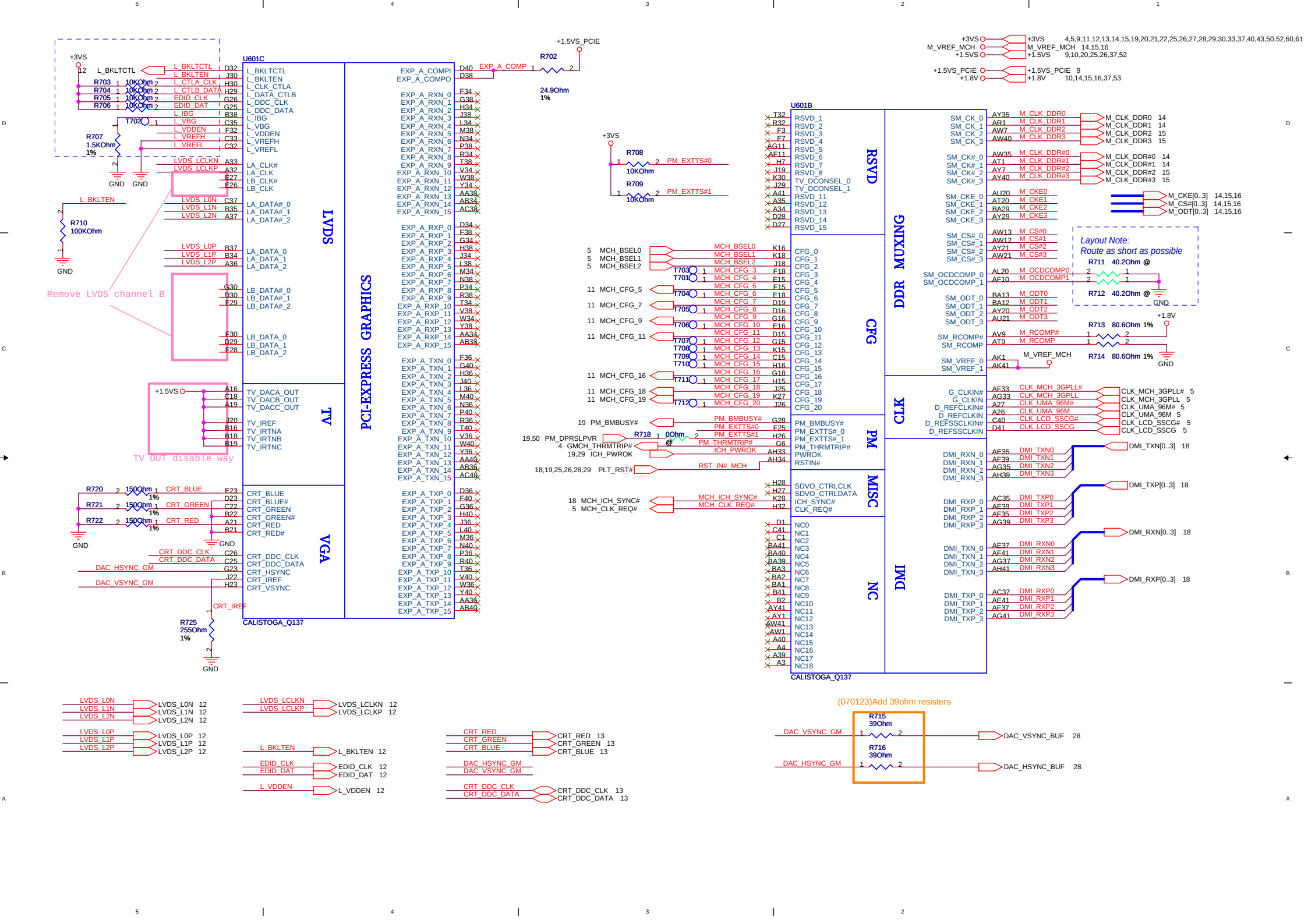
PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

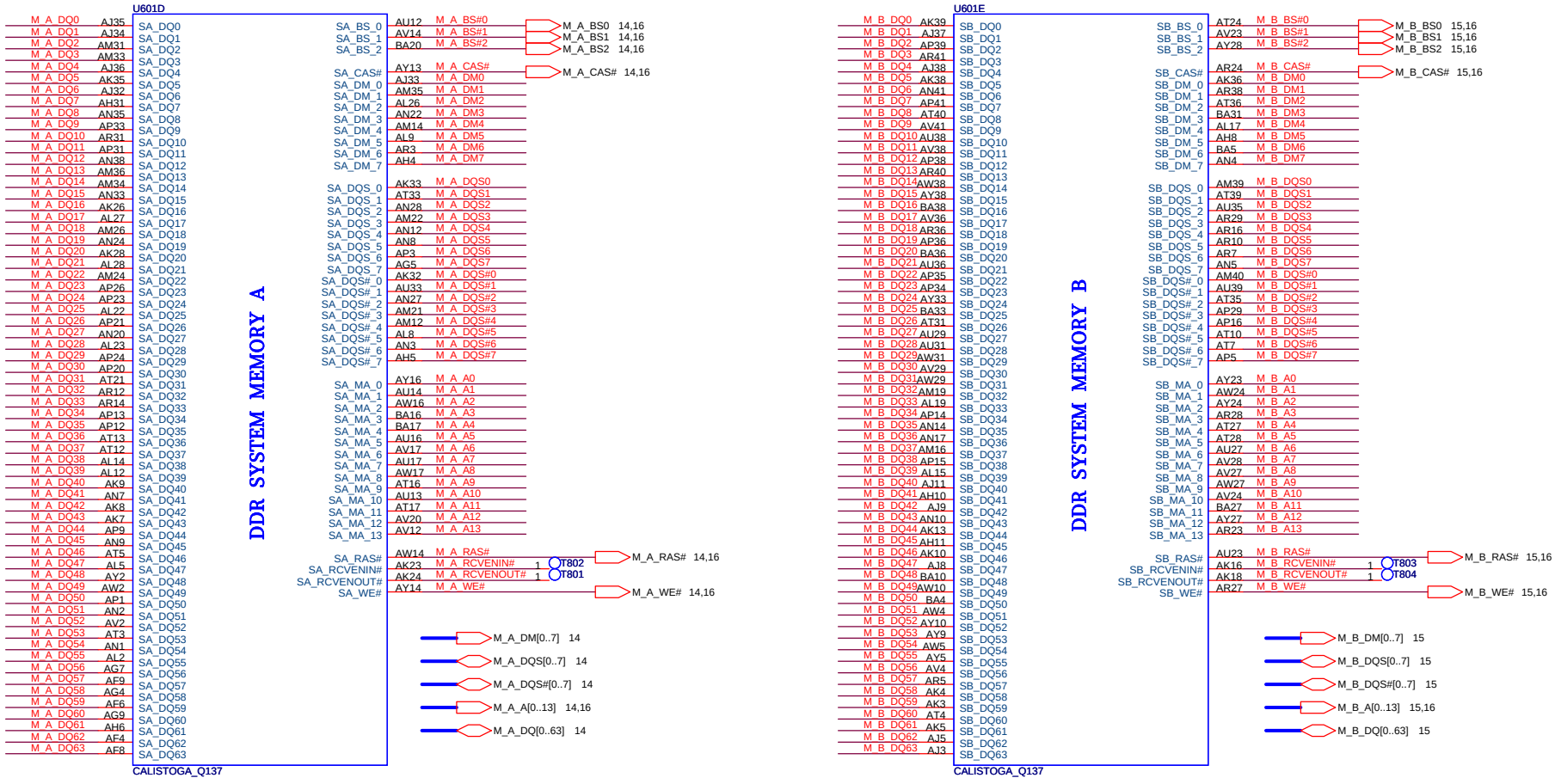
ICS954310CGLFT

Internal Pull-Up Resistor

Internal Pull-Down Resistor


H_D#[0..63] 2
H_A#[31..3] 2
U601A
HOST
CALISTOGA_Q137
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
CLK_MCH_BCLK AG2
CLK_MCH_BCLK# AG1
5 CLK_MCH_BCLK
5 CLK_MCH_BCLK#
H_A#_3 H9 H_A#3
H_A#_4 C9 H_A#4
H_A#_5 E11 H_A#5
H_A#_6 G11 H_A#6
H_A#_7 F11 H_A#7
H_A#_8 G12 H_A#8
H_A#_9 F9 H_A#9
H_A#_10 H11 H_A#10
H_A#_11 J12 H_A#11
H_A#_12 G14 H_A#12
H_A#_13 D9 H_A#13
H_A#_14 J14 H_A#14
H_A#_15 H13 H_A#15
H_A#_16 J15 H_A#16
H_A#_17 F14 H_A#17
H_A#_18 D12 H_A#18
H_A#_19 A11 H_A#19
H_A#_20 C11 H_A#20
H_A#_21 A12 H_A#21
H_A#_22 A13 H_A#22
H_A#_23 E13 H_A#23
H_A#_24 G13 H_A#24
H_A#_25 F12 H_A#25
H_A#_26 B12 H_A#26
H_A#_27 B14 H_A#27
H_A#_28 C12 H_A#28
H_A#_29 A14 H_A#29
H_A#_30 C14 H_A#30
H_A#_31 D14 H_A#31
H_ADS# E8 H_ADS# H_ADS# 2
H_ADSTB#_0 B9 H_ADSTB#0 H_ADSTB#0 2
H_ADSTB#_1 C13 H_ADSTB#1 H_ADSTB#1 2
H_AVREF J13 H_VREF
H_BNR# C6 H_BNR# H_BNR# 2
H_BPRI# F6 H_BPRI# H_BPRI# 2
H_BREQ#0 C7 H_BR0# H_BR0# 2
H_CPURST# B7 H_CPURST# H_CPURST# 2
H_DBSY# A7 H_DBSY# H_DBSY# 2
H_DEFER# C3 H_DEFER# H_DEFER# 2
H_DPWR# J9 H_DPWR# H_DPWR# 2
H_DRDY# H8 H_DRDY# H_DRDY# 2
H_DVREF K13
H_DINV#_0 J7 H_DINV#0 H_DINV#0 2
H_DINV#_1 W8 H_DINV#1 H_DINV#1 2
H_DINV#_2 U3 H_DINV#2 H_DINV#2 2
H_DINV#_3 AB10 H_DINV#3 H_DINV#3 2
H_DSTBN#_0 K4 H_DSTBN#0 H_DSTBN#0 2
H_DSTBN#_1 T7 H_DSTBN#1 H_DSTBN#1 2
H_DSTBN#_2 Y5 H_DSTBN#2 H_DSTBN#2 2
H_DSTBN#_3 AC4 H_DSTBN#3 H_DSTBN#3 2
H_DSTBP#_0 K3 H_DSTBP#0 H_DSTBP#0 2
H_DSTBP#_1 T6 H_DSTBP#1 H_DSTBP#1 2
H_DSTBP#_2 AA5 H_DSTBP#2 H_DSTBP#2 2
H_DSTBP#_3 AC5 H_DSTBP#3 H_DSTBP#3 2
H_HIT# D3 H_HIT# H_HIT# 2
H_HITM# D4 H_HITM# H_HITM# 2
H_LOCK# B3 H_LOCK# H_LOCK# 2
H_REQ#_0 D8 H_REQ#0
H_REQ#_1 G8 H_REQ#1
H_REQ#_2 B8 H_REQ#2
H_REQ#_3 F8 H_REQ#3
H_REQ#_4 A8 H_REQ#4
H_REQ#[4..0] 2
H_RS#_0 B4 H_RS#0
H_RS#_1 E6 H_RS#1
H_RS#_2 D6 H_RS#2
H_RS#[0..2] 2
H_SLPCPU# E3 N_CPUSLP# 2
H_TRDY# E7 H_TRDY#
R611 0Ohm
H_CPUSLP# 2,17
H_TRDY# 2
+VCCP_AGTL+
R601 100Ohm 1%
R606 200Ohm 1%
C601 0.1UF/10V
GND
<500 mil (55 Ohm)
T/B trace 5.5 ,
Space 25
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.
+VCCP +VCCP 2,9,20,52
+VCCP_AGTL+ +VCCP_AGTL+ 2,3,5,9
+VCCP
R602 54.9Ohm 1%
R603 54.9Ohm 1%
5.5/20 mils
H_XSCOMP
H_YSCOMP
H_XRCOMP
H_YRCOMP
R604 24.9Ohm 1%
R605 24.9Ohm 1%
10/20mils
R607 221Ohm 1%
R608 100Ohm 1%
C602 0.1UF/10V
H_XSWING
10/20mils
R609 221Ohm 1%
R610 100Ohm 1%
C603 0.1UF/10V
H_YSWING
Signal voltage level = 0.3125*VCCP
Trace should be 10 mil wide with 20 mil spacing


U601C
CALISTOGA_Q137
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
Remove LVDS channel B
TV OUT disable way
U601B
RSVD
DDR MUXING
CFG
CLK
PM
MISC
DMI
NC
Layout Note:
Route as short as possible
(070123)Add 39ohm resisters


U601D
DDR SYSTEM MEMORY A
CALISTOGA_Q137
M_A_DQ0 AJ35
M_A_DQ1 AJ34
M_A_DQ2 AM31
M_A_DQ3 AM33
M_A_DQ4 AJ36
M_A_DQ5 AK35
M_A_DQ6 AJ32
M_A_DQ7 AH31
M_A_DQ8 AN35
M_A_DQ9 AP33
M_A_DQ10 AR31
M_A_DQ11 AP31
M_A_DQ12 AN38
M_A_DQ13 AM36
M_A_DQ14 AM34
M_A_DQ15 AN33
M_A_DQ16 AK26
M_A_DQ17 AL27
M_A_DQ18 AM26
M_A_DQ19 AN24
M_A_DQ20 AK28
M_A_DQ21 AL28
M_A_DQ22 AM24
M_A_DQ23 AP26
M_A_DQ24 AP23
M_A_DQ25 AL22
M_A_DQ26 AP21
M_A_DQ27 AN20
M_A_DQ28 AL23
M_A_DQ29 AP24
M_A_DQ30 AP20
M_A_DQ31 AT21
M_A_DQ32 AR12
M_A_DQ33 AR14
M_A_DQ34 AP13
M_A_DQ35 AP12
M_A_DQ36 AT13
M_A_DQ37 AT12
M_A_DQ38 AL14
M_A_DQ39 AL12
M_A_DQ40 AK9
M_A_DQ41 AN7
M_A_DQ42 AK8
M_A_DQ43 AK7
M_A_DQ44 AP9
M_A_DQ45 AN9
M_A_DQ46 AT5
M_A_DQ47 AL5
M_A_DQ48 AV2
M_A_DQ49 AW2
M_A_DQ50 AP1
M_A_DQ51 AN2
M_A_DQ52 AV2
M_A_DQ53 AT3
M_A_DQ54 AN1
M_A_DQ55 AL2
M_A_DQ56 AG7
M_A_DQ57 AF9
M_A_DQ58 AG4
M_A_DQ59 AF6
M_A_DQ60 AG9
M_A_DQ61 AH6
M_A_DQ62 AF4
M_A_DQ63 AF8
SA_DQ0
SA_DQ1
SA_DQ2
SA_DQ3
SA_DQ4
SA_DQ5
SA_DQ6
SA_DQ7
SA_DQ8
SA_DQ9
SA_DQ10
SA_DQ11
SA_DQ12
SA_DQ13
SA_DQ14
SA_DQ15
SA_DQ16
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SA_DQ36
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SA_DQ38
SA_DQ39
SA_DQ40
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SA_DQ42
SA_DQ43
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SA_DQ53
SA_DQ54
SA_DQ55
SA_DQ56
SA_DQ57
SA_DQ58
SA_DQ59
SA_DQ60
SA_DQ61
SA_DQ62
SA_DQ63
SA_BS_0
SA_BS_1
SA_BS_2
SA_CAS#
SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7
SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7
SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7
SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_RAS#
SA_RCVENIN#
SA_RCVENOUT#
SA_WE#
AU12 M_A_BS#0
AV14 M_A_BS#1
BA20 M_A_BS#2
AY13 M_A_CAS#
AJ33 M_A_DM0
AM35 M_A_DM1
AL26 M_A_DM2
AN22 M_A_DM3
AM14 M_A_DM4
AL9 M_A_DM5
AR3 M_A_DM6
AH4 M_A_DM7
AK33 M_A_DQS0
AT33 M_A_DQS1
AN28 M_A_DQS2
AM22 M_A_DQS3
AN12 M_A_DQS4
AN8 M_A_DQS5
AP3 M_A_DQS6
AG5 M_A_DQS7
AK32 M_A_DQS#0
AU33 M_A_DQS#1
AN27 M_A_DQS#2
AM21 M_A_DQS#3
AM12 M_A_DQS#4
AL8 M_A_DQS#5
AN3 M_A_DQS#6
AH5 M_A_DQS#7
AY16 M_A_A0
AU14 M_A_A1
AW16 M_A_A2
BA16 M_A_A3
BA17 M_A_A4
AU16 M_A_A5
AV17 M_A_A6
AU17 M_A_A7
AW17 M_A_A8
AT16 M_A_A9
AU13 M_A_A10
AT17 M_A_A11
AV20 M_A_A12
AV12 M_A_A13
AW14 M_A_RAS#
AK23 M_A_RCVENIN# 1 T802
AK24 M_A_RCVENOUT# 1 T801
AY14 M_A_WE#
M_A_BS0 14,16
M_A_BS1 14,16
M_A_BS2 14,16
M_A_CAS# 14,16
M_A_RAS# 14,16
M_A_WE# 14,16
M_A_DM[0..7] 14
M_A_DQS[0..7] 14
M_A_DQS#[0..7] 14
M_A_A[0..13] 14,16
M_A_DQ[0..63] 14
U601E
DDR SYSTEM MEMORY B
CALISTOGA_Q137
M_B_DQ0 AK39
M_B_DQ1 AJ37
M_B_DQ2 AP39
M_B_DQ3 AR41
M_B_DQ4 AJ38
M_B_DQ5 AK38
M_B_DQ6 AN41
M_B_DQ7 AP41
M_B_DQ8 AT40
M_B_DQ9 AV41
M_B_DQ10 AU38
M_B_DQ11 AV38
M_B_DQ12 AP38
M_B_DQ13 AR40
M_B_DQ14 AW38
M_B_DQ15 AY38
M_B_DQ16 BA38
M_B_DQ17 AV36
M_B_DQ18 AR36
M_B_DQ19 AP36
M_B_DQ20 BA36
M_B_DQ21 AU36
M_B_DQ22 AP35
M_B_DQ23 AP34
M_B_DQ24 AY33
M_B_DQ25 BA33
M_B_DQ26 AT31
M_B_DQ27 AU29
M_B_DQ28 AU31
M_B_DQ29 AW31
M_B_DQ30 AV29
M_B_DQ31 AW29
M_B_DQ32 AM19
M_B_DQ33 AL19
M_B_DQ34 AP14
M_B_DQ35 AN14
M_B_DQ36 AN17
M_B_DQ37 AM16
M_B_DQ38 AP15
M_B_DQ39 AL15
M_B_DQ40 AJ11
M_B_DQ41 AH10
M_B_DQ42 AJ9
M_B_DQ43 AN10
M_B_DQ44 AK13
M_B_DQ45 AH11
M_B_DQ46 AK10
M_B_DQ47 AJ8
M_B_DQ48 BA10
M_B_DQ49 AW10
M_B_DQ50 BA4
M_B_DQ51 AW4
M_B_DQ52 AY10
M_B_DQ53 AY9
M_B_DQ54 AW5
M_B_DQ55 AY5
M_B_DQ56 AV4
M_B_DQ57 AR5
M_B_DQ58 AK4
M_B_DQ59 AK3
M_B_DQ60 AT4
M_B_DQ61 AK5
M_B_DQ62 AJ5
M_B_DQ63 AJ3
SB_DQ0
SB_DQ1
SB_DQ2
SB_DQ3
SB_DQ4
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SB_DM_7
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SB_DQS_1
SB_DQS_2
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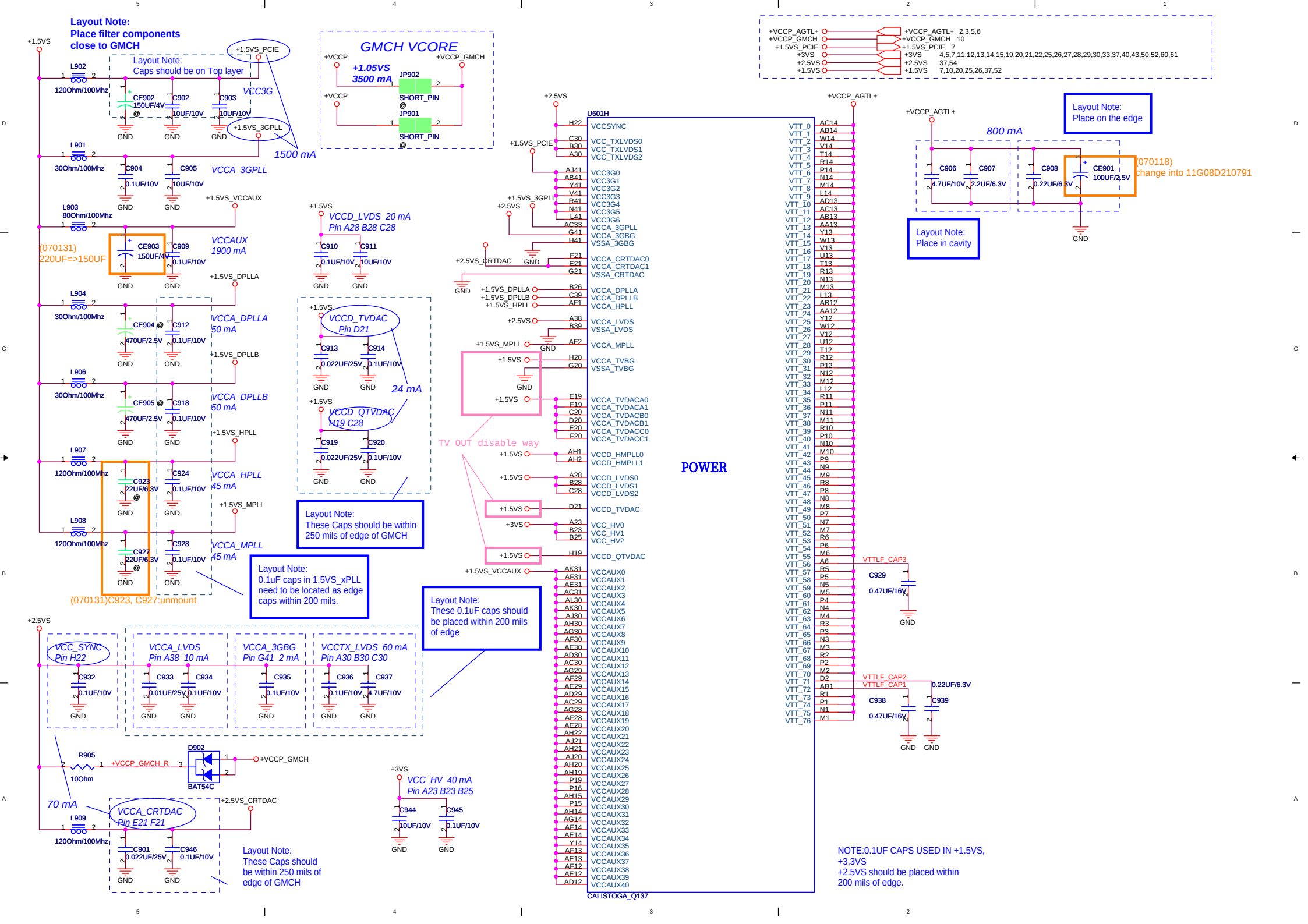
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_RAS#
SB_RCVENIN#
SB_RCVENOUT#
SB_WE#
AT24 M_B_BS#0
AV23 M_B_BS#1
AY28 M_B_BS#2
AR24 M_B_CAS#
AK36 M_B_DM0
AR38 M_B_DM1
AT36 M_B_DM2
BA31 M_B_DM3
AL17 M_B_DM4
AH8 M_B_DM5
BA5 M_B_DM6
AN4 M_B_DM7
AM39 M_B_DQS0
AT39 M_B_DQS1
AU35 M_B_DQS2
AR29 M_B_DQS3
AR16 M_B_DQS4
AR10 M_B_DQS5
AR7 M_B_DQS6
AN5 M_B_DQS7
AM40 M_B_DQS#0
AU39 M_B_DQS#1
AT35 M_B_DQS#2
AP29 M_B_DQS#3
AP16 M_B_DQS#4
AT10 M_B_DQS#5
AT7 M_B_DQS#6
AP5 M_B_DQS#7
AY23 M_B_A0
AW24 M_B_A1
AY24 M_B_A2
AR28 M_B_A3
AT27 M_B_A4
AT28 M_B_A5
AU27 M_B_A6
AV28 M_B_A7
AV27 M_B_A8
AW27 M_B_A9
AV24 M_B_A10
BA27 M_B_A11
AY27 M_B_A12
AR23 M_B_A13
AU23 M_B_RAS#
AK16 M_B_RCVENIN# 1 T803
AK18 M_B_RCVENOUT# 1 T804
AR27 M_B_WE#
M_B_BS0 15,16
M_B_BS1 15,16
M_B_BS2 15,16
M_B_CAS# 15,16
M_B_RAS# 15,16
M_B_WE# 15,16
M_B_DM[0..7] 15
M_B_DQS[0..7] 15
M_B_DQS#[0..7] 15
M_B_A[0..13] 15,16
M_B_DQ[0..63] 15


Layout Note:
Place filter components
close to GMCH
+1.5VS
L902
120Ohm/100Mhz
Layout Note:
Caps should be on Top layer
+1.5VS_PCIE
VCC3G
CE902
150UF/4V
@
C902
10UF/10V
C903
10UF/10V
GND
+1.5VS_3GPLL
1500 mA
L901
30Ohm/100Mhz
C904
0.1UF/10V
C905
10UF/10V
VCCA_3GPLL
+1.5VS_VCCAUX
L903
80Ohm/100Mhz
(070131)
220UF=>150UF
CE903
150UF/4V
C909
0.1UF/10V
VCCAUX
1900 mA
+1.5VS_DPLLA
L904
30Ohm/100Mhz
CE904 @
470UF/2.5V
C912
0.1UF/10V
VCCA_DPLLA
50 mA
+1.5VS_DPLLB
L906
30Ohm/100Mhz
CE905 @
470UF/2.5V
C918
0.1UF/10V
VCCA_DPLLB
50 mA
+1.5VS_HPLL
L907
120Ohm/100Mhz
C923
22UF/6.3V
@
C924
0.1UF/10V
VCCA_HPLL
45 mA
+1.5VS_MPLL
L908
120Ohm/100Mhz
C927
22UF/6.3V
@
C928
0.1UF/10V
VCCA_MPLL
45 mA
(070131)C923, C927:unmount
GMCH VCORE
+VCCP
+1.05VS
3500 mA
+VCCP_GMCH
JP902
SHORT_PIN
@
JP901
SHORT_PIN
@
+VCCP_AGTL+
+VCCP_GMCH
+1.5VS_PCIE
+3VS
+2.5VS
+1.5VS
+VCCP_AGTL+ 2,3,5,6
+VCCP_GMCH 10
+1.5VS_PCIE 7
+3VS 4,5,7,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61
+2.5VS 37,54
+1.5VS 7,10,20,25,26,37,52
+1.5VS
VCCD_LVDS 20 mA
Pin A28 B28 C28
C910
0.1UF/10V
C911
10UF/10V
+1.5VS
VCCD_TVDAC
Pin D21
C913
0.022UF/25V
C914
0.1UF/10V
24 mA
+1.5VS
VCCD_QTVDAC
H19 C28
C919
0.022UF/25V
C920
0.1UF/10V
Layout Note:
These Caps should be within
250 mils of edge of GMCH
Layout Note:
0.1uF caps in 1.5VS_xPLL
need to be located as edge
caps within 200 mils.
Layout Note:
These 0.1uF caps should
be placed within 200 mils
of edge
+2.5VS
VCC_SYNC
Pin H22
C932
0.1UF/10V
VCCA_LVDS
Pin A38 10 mA
C933
0.01UF/25V
C934
0.1UF/10V
VCCA_3GBG
Pin G41 2 mA
C935
0.1UF/10V
VCCTX_LVDS 60 mA
Pin A30 B30 C30
C936
0.1UF/10V
C937
4.7UF/10V
R905
10Ohm
+VCCP_GMCH_R
D902
BAT54C
+VCCP_GMCH
70 mA
VCCA_CRTDAC
Pin E21 F21
+2.5VS_CRTDAC
L909
120Ohm/100Mhz
C901
0.022UF/25V
C946
0.1UF/10V
Layout Note:
These Caps should
be within 250 mils of
edge of GMCH
+3VS
VCC_HV 40 mA
Pin A23 B23 B25
C944
10UF/10V
C945
0.1UF/10V
U601H
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
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VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
CALISTOGA_Q137
TV OUT disable way
POWER
+VCCP_AGTL+
VTT_0
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
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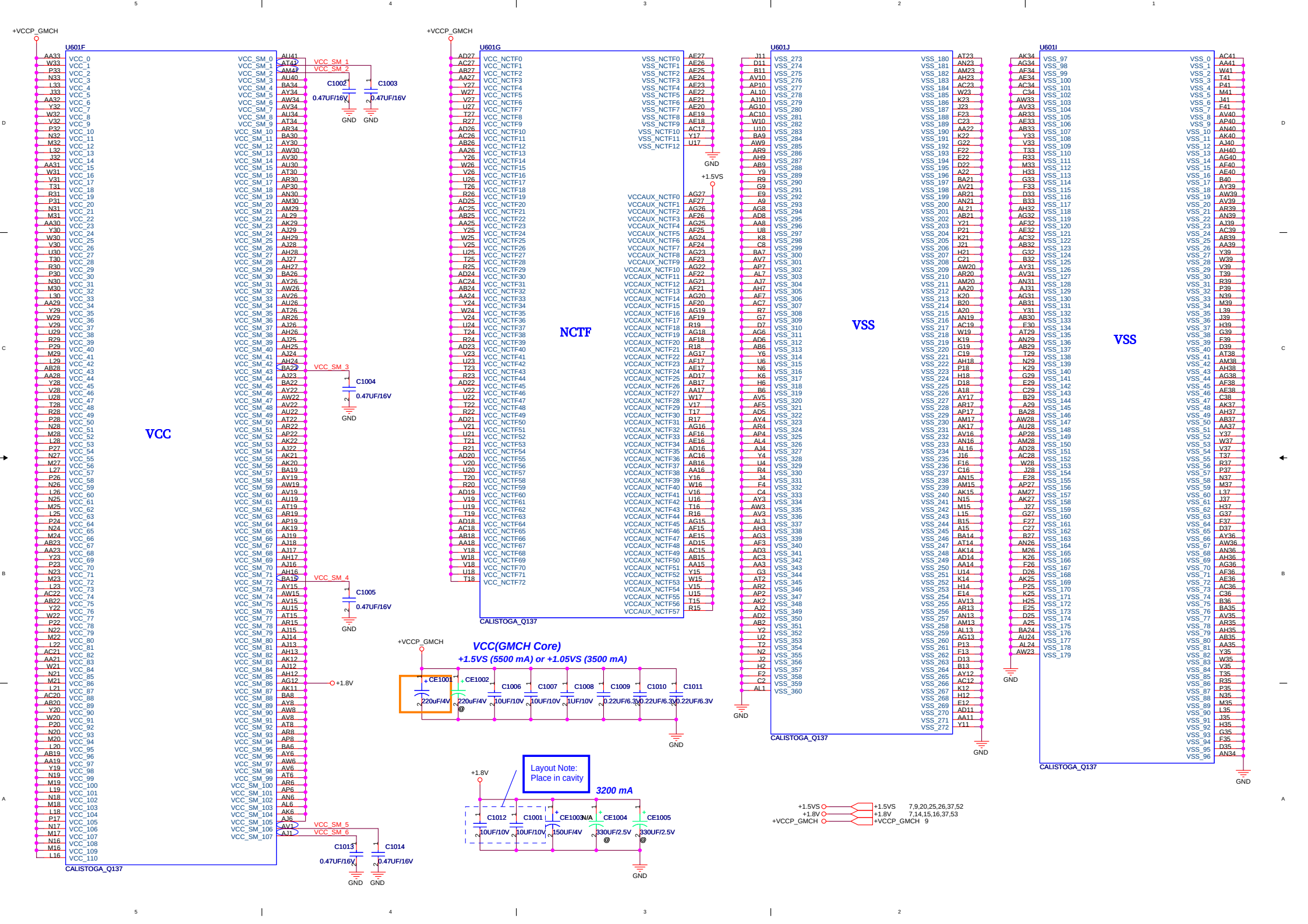
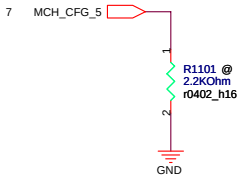
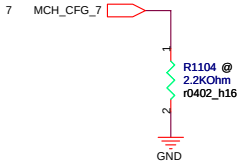
VTT_65
VTT_66
VTT_67
VTT_68
VTT_69
VTT_70
VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
VTTLF_CAP3
C929
0.47UF/16V
VTTLF_CAP2
VTTLF_CAP1
C938
0.47UF/16V
C939
0.22UF/6.3V
+VCCP_AGTL+
800 mA
Layout Note:
Place on the edge
C906
4.7UF/10V
C907
2.2UF/6.3V
C908
0.22UF/6.3V
CE901
100UF/2.5V
(070118)
change into 11G08D210791
Layout Note:
Place in cavity
NOTE:0.1UF CAPS USED IN +1.5VS,
+3.3VS
+2.5VS should be placed within
200 mils of edge.

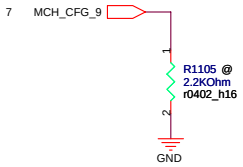

U601F
VCC
CALISTOGA_Q137
U601G
NCTF
CALISTOGA_Q137
U601J
VSS
CALISTOGA_Q137
U601I
VSS
CALISTOGA_Q137
+VCCP_GMCH
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
C1002
C1003
C1004
C1005
C1013
C1014
0.47UF/16V
GND
+1.8V
+1.5VS
VCC(GMCH Core)
+1.5VS (5500 mA) or +1.05VS (3500 mA)
CE1001
CE1002
C1006
C1007
C1008
C1009
C1010
C1011
220uF/4V
220uF/4V
10UF/10V
10UF/10V
1UF/10V
0.22UF/6.3V
0.22UF/6.3V
0.22UF/6.3V
Layout Note:
Place in cavity
3200 mA
C1012
C1001
CE1003
N/A
CE1004
CE1005
10UF/10V
10UF/10V
150UF/4V
330UF/2.5V
330UF/2.5V
+1.5VS 7,9,20,25,26,37,52
+1.8V 7,14,15,16,37,53
+VCCP_GMCH 9



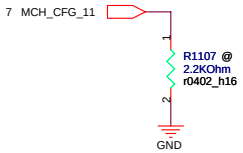
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



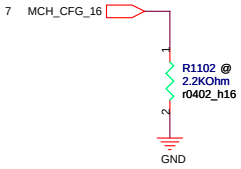
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



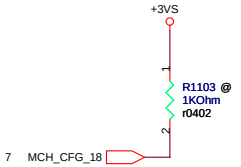
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



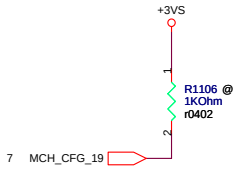
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



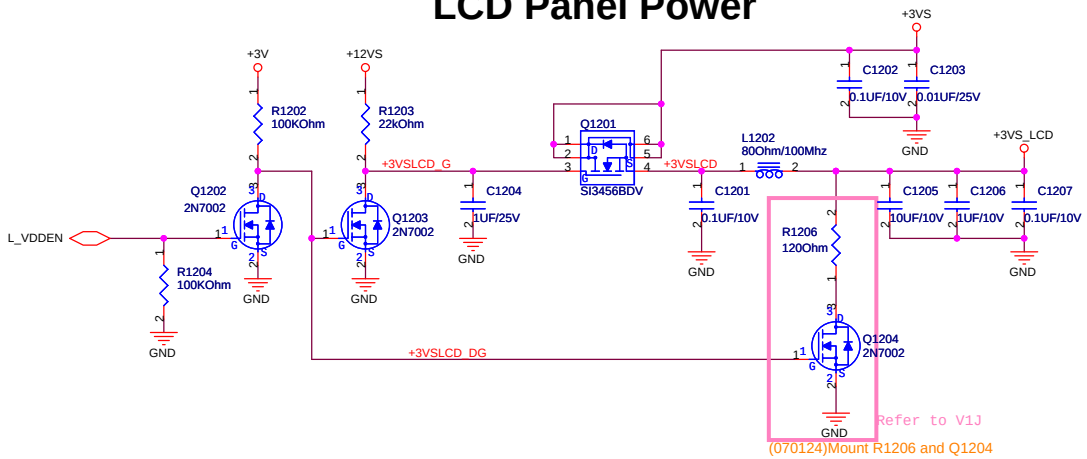
CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)

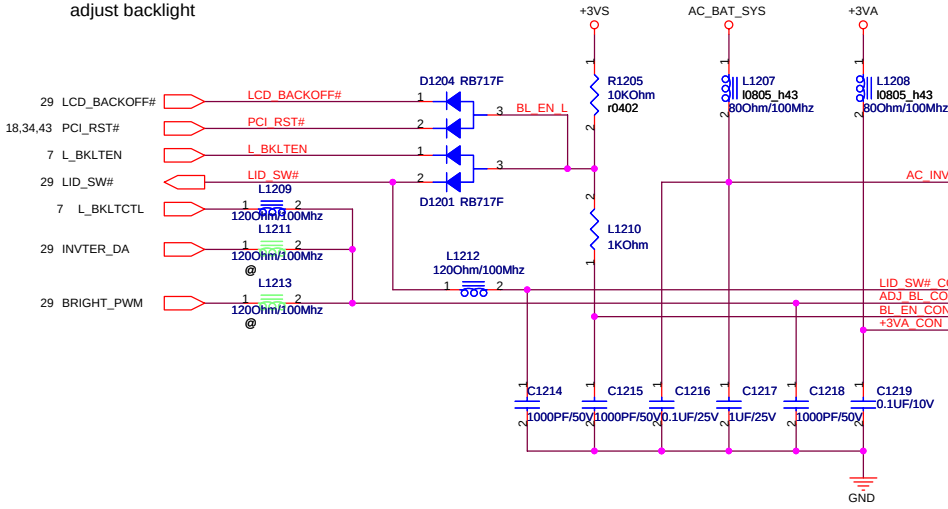


LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 15.4W LCD Panel



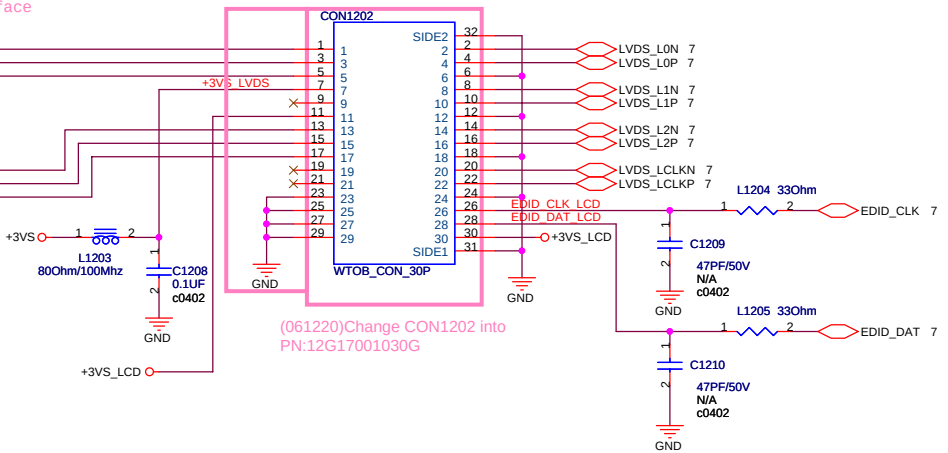
Combine Inverter interface into LVDS interface

(061206,EMI)
Add bead

LCD LVDS & INVERTER Interface

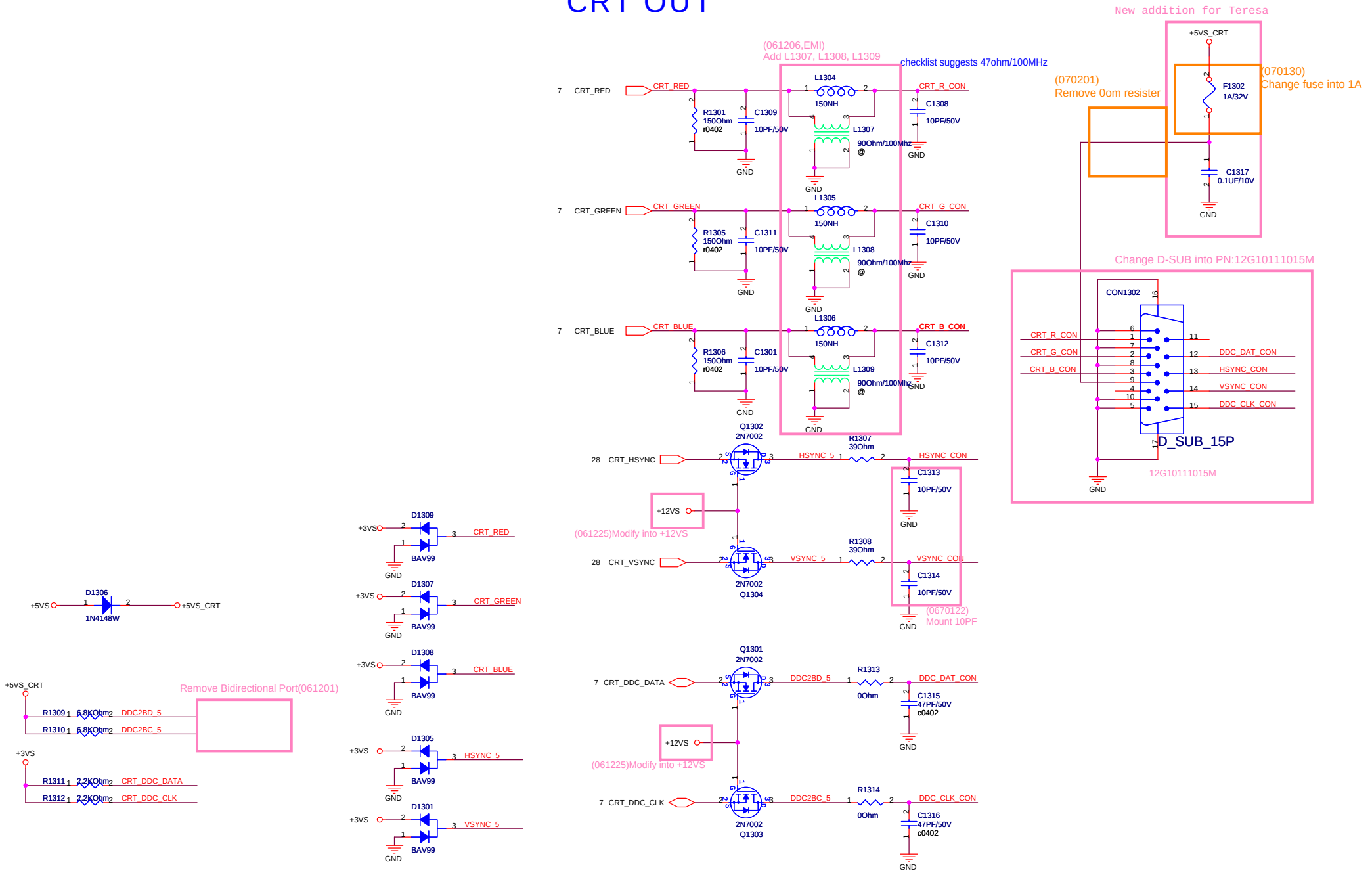
Delete LVDS channel B

Rearrange pin location(061201)

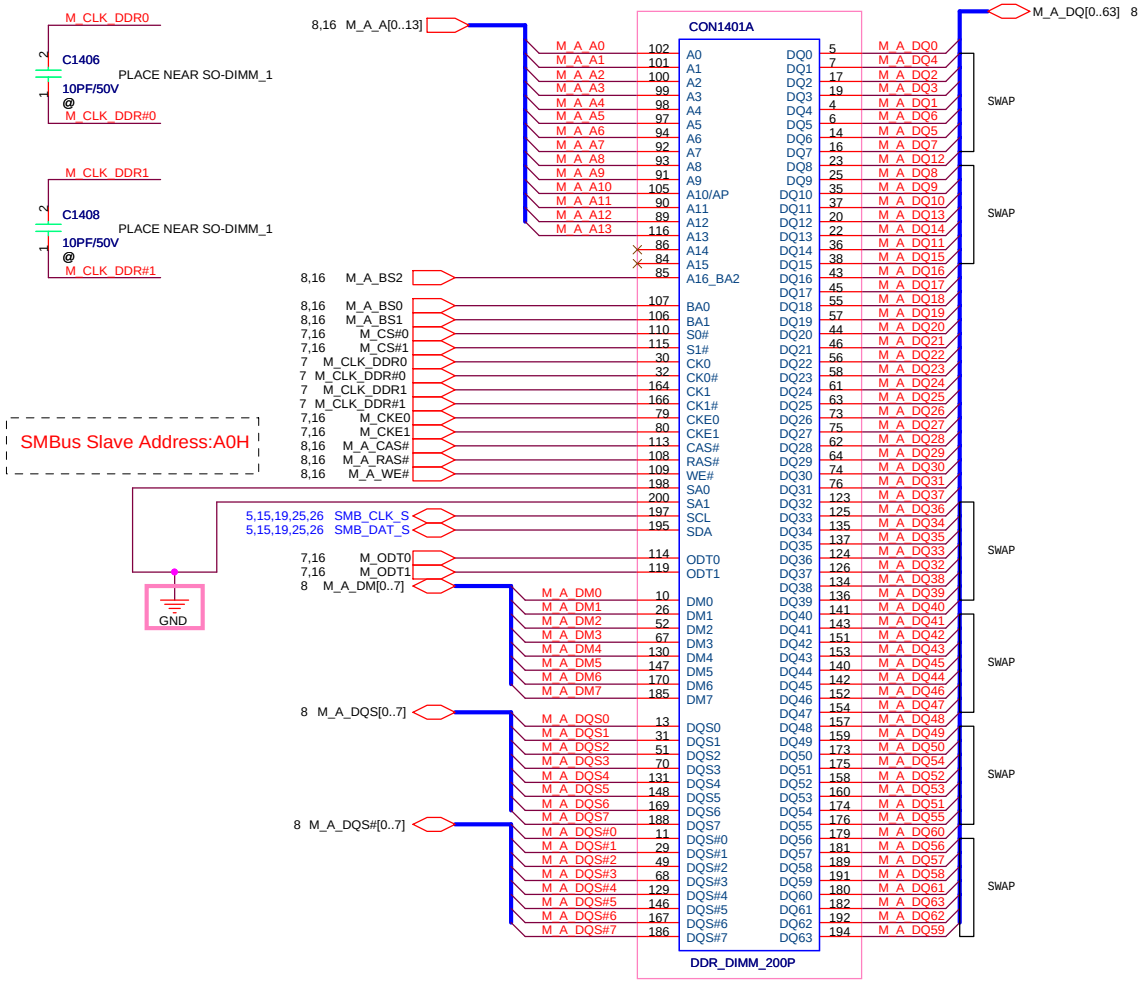


(061220)Change CON1202 into PN:12G17001030G

CRT OUT

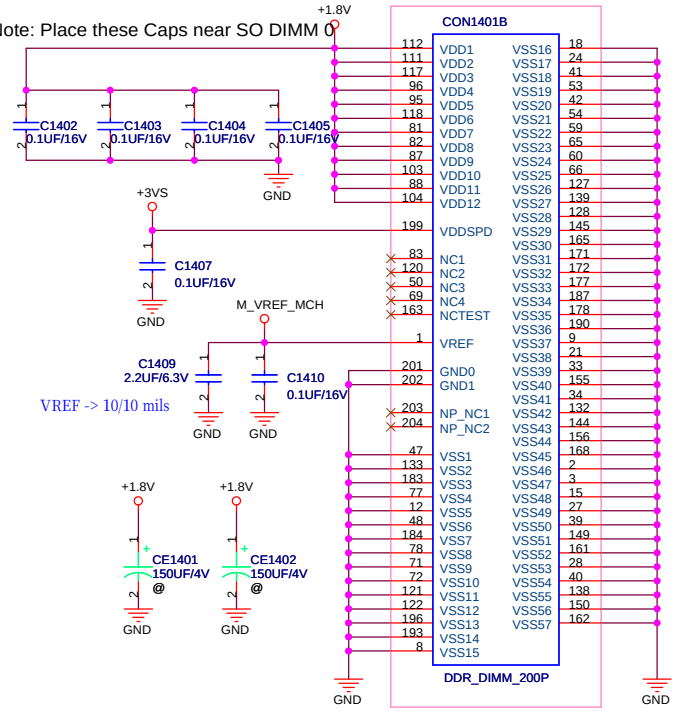

(061206,EMI)
Add L1307, L1308, L1309
checklist suggests 47ohm/100MHz
CRT_RED
CRT_GREEN
CRT_BLUE
R1301 150Ohm r0402
R1305 150Ohm r0402
R1306 150Ohm r0402
C1309 10PF/50V
C1311 10PF/50V
C1301 10PF/50V
L1304 150NH
L1305 150NH
L1306 150NH
L1307 90Ohm/100Mhz @
L1308 90Ohm/100Mhz @
L1309 90Ohm/100Mhz @
CRT_R_CON
CRT_G_CON
CRT_B_CON
C1308 10PF/50V
C1310 10PF/50V
C1312 10PF/50V
GND
Q1302 2N7002
Q1304 2N7002
Q1301 2N7002
Q1303 2N7002
CRT_HSYNC
CRT_VSYNC
CRT_DDC_DATA
CRT_DDC_CLK
R1307 39Ohm
R1308 39Ohm
R1313 0Ohm
R1314 0Ohm
HSYNC_5
VSYNC_5
DDC2BD_5
DDC2BC_5
HSYNC_CON
VSYNC_CON
DDC_DAT_CON
DDC_CLK_CON
C1313 10PF/50V
C1314 10PF/50V
C1315 47PF/50V c0402
C1316 47PF/50V c0402
+12VS
(061225)Modify into +12VS
(0670122)
Mount 10PF
New addition for Teresa
(070201)
Remove 0om resister
+5VS_CRT
F1302 1A/32V
(070130)
Change fuse into 1A
C1317 0.1UF/10V
Change D-SUB into PN:12G10111015M
CON1302
D_SUB_15P
12G10111015M
D1306 1N4148W
+5VS
Remove Bidirectional Port(061201)
R1309 6.8KOhm
R1310 6.8KOhm
R1311 2.2KOhm
R1312 2.2KOhm
+3VS
D1309
D1307
D1308
D1305
D1301
BAV99

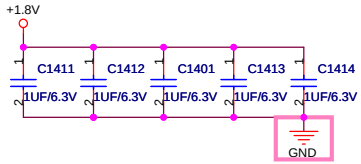
(061221)Change CON1401 into PN:12G02502200R

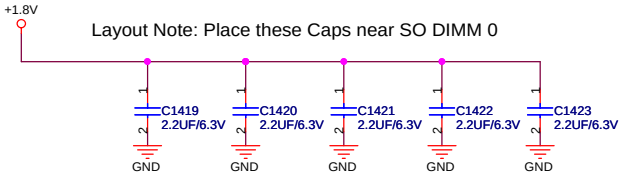


Layout Note: Place these Caps near SO DIMM 0

(061221)Change CON1401 into PN:12G02502200R

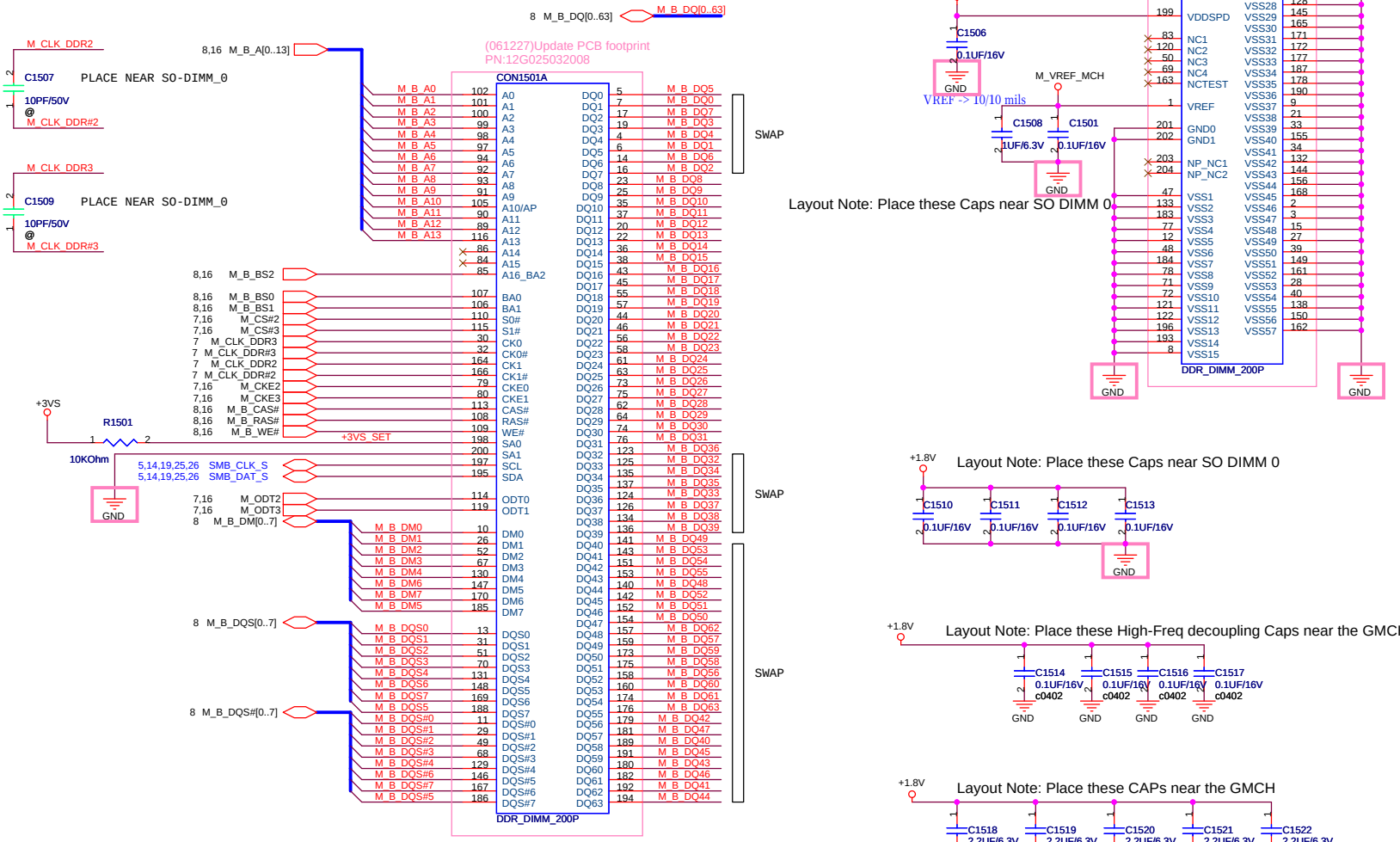




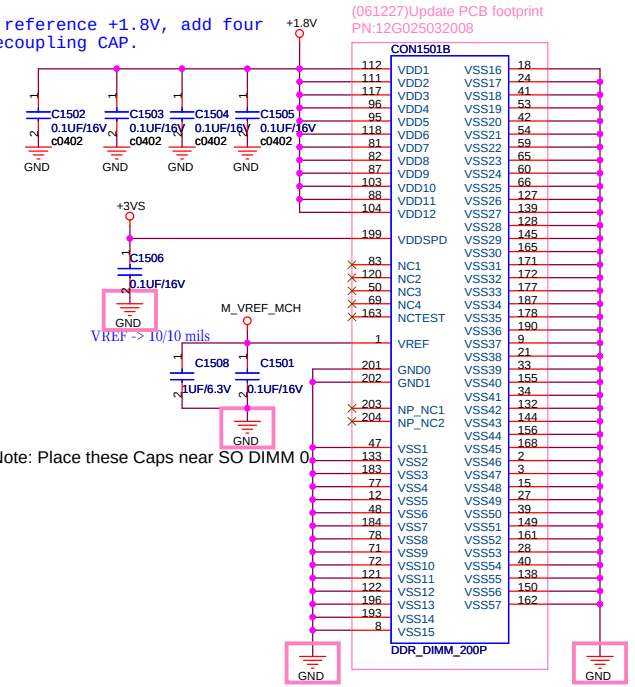


SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

SMBus Slave Address:A4H



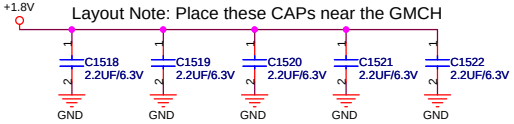
Address reference +1.8V, add four 0.1uF decoupling CAP.

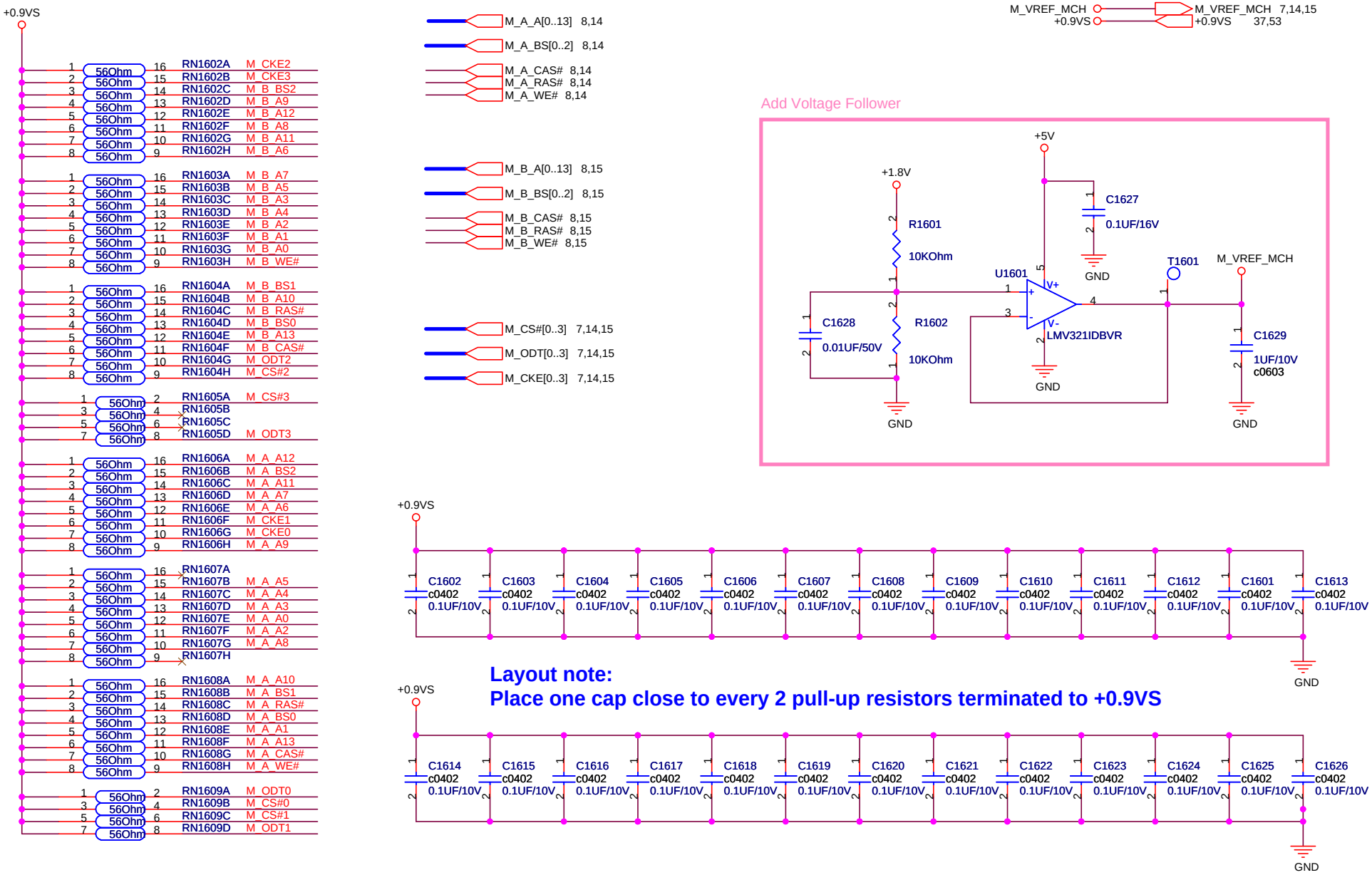


Layout Note: Place these Caps near SO DIMM 0

Layout Note: Place these High-Freq decoupling Caps near the GMCH

Layout Note: Place these CAPs near the GMCH




+0.9VS
RN1602A M_CKE2
RN1602B M_CKE3
RN1602C M_B_BS2
RN1602D M_B_A9
RN1602E M_B_A12
RN1602F M_B_A8
RN1602G M_B_A11
RN1602H M_B_A6
RN1603A M_B_A7
RN1603B M_B_A5
RN1603C M_B_A3
RN1603D M_B_A4
RN1603E M_B_A2
RN1603F M_B_A1
RN1603G M_B_A0
RN1603H M_B_WE#
RN1604A M_B_BS1
RN1604B M_B_A10
RN1604C M_B_RAS#
RN1604D M_B_BS0
RN1604E M_B_A13
RN1604F M_B_CAS#
RN1604G M_ODT2
RN1604H M_CS#2
RN1605A M_CS#3
RN1605B
RN1605C
RN1605D M_ODT3
RN1606A M_A_A12
RN1606B M_A_BS2
RN1606C M_A_A11
RN1606D M_A_A7
RN1606E M_A_A6
RN1606F M_CKE1
RN1606G M_CKE0
RN1606H M_A_A9
RN1607A
RN1607B M_A_A5
RN1607C M_A_A4
RN1607D M_A_A3
RN1607E M_A_A0
RN1607F M_A_A2
RN1607G M_A_A8
RN1607H
RN1608A M_A_A10
RN1608B M_A_BS1
RN1608C M_A_RAS#
RN1608D M_A_BS0
RN1608E M_A_A1
RN1608F M_A_A13
RN1608G M_A_CAS#
RN1608H M_A_WE#
RN1609A M_ODT0
RN1609B M_CS#0
RN1609C M_CS#1
RN1609D M_ODT1
56Ohm
M_A_A[0..13] 8,14
M_A_BS[0..2] 8,14
M_A_CAS# 8,14
M_A_RAS# 8,14
M_A_WE# 8,14
M_B_A[0..13] 8,15
M_B_BS[0..2] 8,15
M_B_CAS# 8,15
M_B_RAS# 8,15
M_B_WE# 8,15
M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15
M_VREF_MCH
+0.9VS
M_VREF_MCH 7,14,15
+0.9VS 37,53
Add Voltage Follower
+5V
+1.8V
R1601
10KOhm
C1627
0.1UF/16V
GND
U1601
V+
V-
LMV321IDBVR
T1601
M_VREF_MCH
C1628
0.01UF/50V
R1602
10KOhm
C1629
1UF/10V
c0603
GND
C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1601 C1613
c0402
0.1UF/10V
C1614 C1615 C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624 C1625 C1626
Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

+VCC_RTC
R1701 2 1 RTCRST#
20KOhm
C1704 1UF/16V
JRST1 1 2 2 @
GND

(061227)Change reference from JRST1701 to JRST1

C1702 18PF/50V
X1701 SIDE 1 2 3
C1703 18PF/50V
32.768KHZ
RTC_X1
R1702 10MOhm
RTC_X2
GND

+1.5VS_PCIE_ICH +1.5VS_PCIE_ICH 18,20
+VCCP_ICH +VCCP_ICH 20
+VCC_RTC +VCC_RTC 20
+VCCP +VCCP 2,6,9,20,52
+1.5VS +1.5VS 7,9,10,20,25,26,37,52
+5VS +5VS 4,13,19,20,21,22,28,29,30,34,37,38,50,61
+3VS +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61
+3VA +3VA 4,12,22,29,37,38,40,41,54,59,63

Delete LPC interface of TPM

LPC_AD0_ICH R1728 33Ohm LPC_AD0 LPC_AD0 26,29
LPC_AD1_ICH R1720 33Ohm LPC_AD1 LPC_AD1 26,29
LPC_AD2_ICH R1722 33Ohm LPC_AD2 LPC_AD2 26,29
LPC_AD3_ICH R1724 33Ohm LPC_AD3 LPC_AD3 26,29
LPC_FRAME#_ICH R1726 33Ohm LPC_FRAME# LPC_FRAME# 26,29

close to ICH7

R1708 39Ohm
21 ACZ_BCLK_AUD
35 ACZ_BCLK_MDC
ACZ_BCLK
R1732 39Ohm

R1710 39Ohm
21 ACZ_SYNC_AUD
35 ACZ_SYNC_MDC
ACZ_SYNC
R1731 39Ohm

R1714 39Ohm
21,22 ACZ_RST#_AUD
ACZ_RST#
R1729 39Ohm
35 ACZ_RST#_MDC

R1717 39Ohm
21 ACZ_SDOUT_AUD
ACZ_SDOUT
R1730 39Ohm
35 ACZ_SDOUT_MDC

U1701A

+VCC_RTC
R1703 1MOhm
R1704 330KOhm
RTC_X1 AB1
RTC_X2 AB2
RTCRST# AA3
INTRUDER# Y5
INTVRMEN W4
RTC

EE_CS W1
EE_SHCLK Y1
EE_DOUT Y2
EE_DIN W3
LAN_CLK V3
LAN_RSTSYNC U3
LAN_RXD0 U5
LAN_RXD1 V4
LAN_RXD2 T5
LAN_TXD0 U7
LAN_TXD1 V6
LAN_TXD2 V7
LAN

ACZ_BCLK U1
ACZ_SYNC R6
ACZ_RST# R5
ACZ_SDIN0 T2
ACZ_SDIN1 T3
ACZ_SDIN2 T1
ACZ_SDOUT T4
21 ACZ_SDIN0
35 ACZ_SDIN1
T1703
AC-97/AZALIA

30 SATA_LED# AF18
SATA_RXN0 AF3
SATA_RXP0 AF3
SATA_TXN0 AG2
SATA_TXP0 AH2
C1705 3900PF/50V SATA_TXN0_ICH
C1701 3900PF/50V SATA_TXP0_ICH
Change to 3900PF
Remove 0 ohm
SATA2_R AE7
SATA2_TN AG6
SATA2_TP AH6
T1704
T1705
GND
5 CLK_PCIE_SATA# AE1
5 CLK_PCIE_SATA AE1
R1719 24.9Ohm 1% SATA2_RBIAS AH10 AG10
GND
SATA

28 IDE_PDIOR# IDE_PDIOR#_ICH AF15
28 IDE_PDIOW# IDE_PDIOW# AH15
28 IDE_PDDACK# IDE_PDDACK# AF16
28 INT_IRQ14 INT_IRQ14 AH16
28 IDE_PIORDY IDE_PIORDY AG16
28 IDE_PDDREQ IDE_PDDREQ AE15
IDE

ICH7M

LAD0 AA6 LPC_AD0_ICH
LAD1 AB5 LPC_AD1_ICH
LAD2 AC4 LPC_AD2_ICH
LAD3 Y6 LPC_AD3_ICH
LDRQ0# AC3 LPC_DRQ#0 LPC_DRQ#0 19
LDRQ1#/GPIO23 AA5 LPC_DRQ#1
T1702
LFRAME# AB3 LPC_FRAME#_ICH

A20GATE AE22 A20GATE A20GATE 29
A20M# AH28 H_A20M# H_A20M# 2
CPUSLP# AG27 S_CPUSLP# R1705 @ 0Ohm H_CPUSLP# 2,6
TP1/DPRSTP# AE24 S_DPRSTP# R1707 @ 0Ohm H_DPRSTP# 2,60
TP2/DPSLP# AH25 H_DPSLP# H_DPSLP# 2
FERR# AG26 H_FERR# H_FERR# 2
GPIO49/CPUPWRGD AG24 H_PWRGD H_PWRGD 2
+VCCP_ICH
R1706 56Ohm

IGNNE# AG22 H_IGNNE# H_IGNNE# 2
INIT3_3V# AG21 INIT3_3V#
INIT# AE22 H_INIT# H_INIT# 2
INTR AE25 H_INTR H_INTR 2
T1701
RCIN# AG23 RCIN# RCIN# 29
NMI AH24 H_NMI H_NMI 2
SMI# AF23 H_SMI# H_SMI# 2
STPCLK# AH22 H_STPCLK# H_STPCLK# 2
THERMTRIP# AF26 S_THRMTRIP# R1713 24.9Ohm 1% PM_THRMTRIP# 2,4
+VCCP_ICH
R1711 56Ohm
CPU

DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ±5% series termination resistor placed within 2" from Intel 82801GBM, 56 ±5% pull-up resistor has to be within 2" from the series resistor

DD0 AB15 IDE_PDD0 IDE_PDD0 28
DD1 AE14 IDE_PDD1_ICH IDE_PDD1 28
DD2 AG13 IDE_PDD2_ICH IDE_PDD2 28
DD3 AF13 IDE_PDD3 IDE_PDD3 28
DD4 AD14 IDE_PDD4 IDE_PDD4 28
DD5 AC13 IDE_PDD5 IDE_PDD5 28
DD6 AD12 IDE_PDD6 IDE_PDD6 28
DD7 AC12 IDE_PDD7 IDE_PDD7 28
DD8 AE12 IDE_PDD8 IDE_PDD8 28
DD9 AF12 IDE_PDD9_ICH IDE_PDD9 28
DD10 AB13 IDE_PDD10_ICH IDE_PDD10 28
DD11 AC14 IDE_PDD11 IDE_PDD11 28
DD12 AE14 IDE_PDD12 IDE_PDD12 28
DD13 AH13 IDE_PDD13 IDE_PDD13 28
DD14 AH14 IDE_PDD14 IDE_PDD14 28
DD15 AC15 IDE_PDD15 IDE_PDD15 28
DA0 AH17 IDE_PDA0 IDE_PDA0 28
DA1 AE17 IDE_PDA1 IDE_PDA1 28
DA2 AF17 IDE_PDA2 IDE_PDA2 28
DCS1# AE16 IDE_PDCS1# IDE_PDCS1# 28
DCS3# AD16 IDE_PDCS3# IDE_PDCS3# 28
IDE

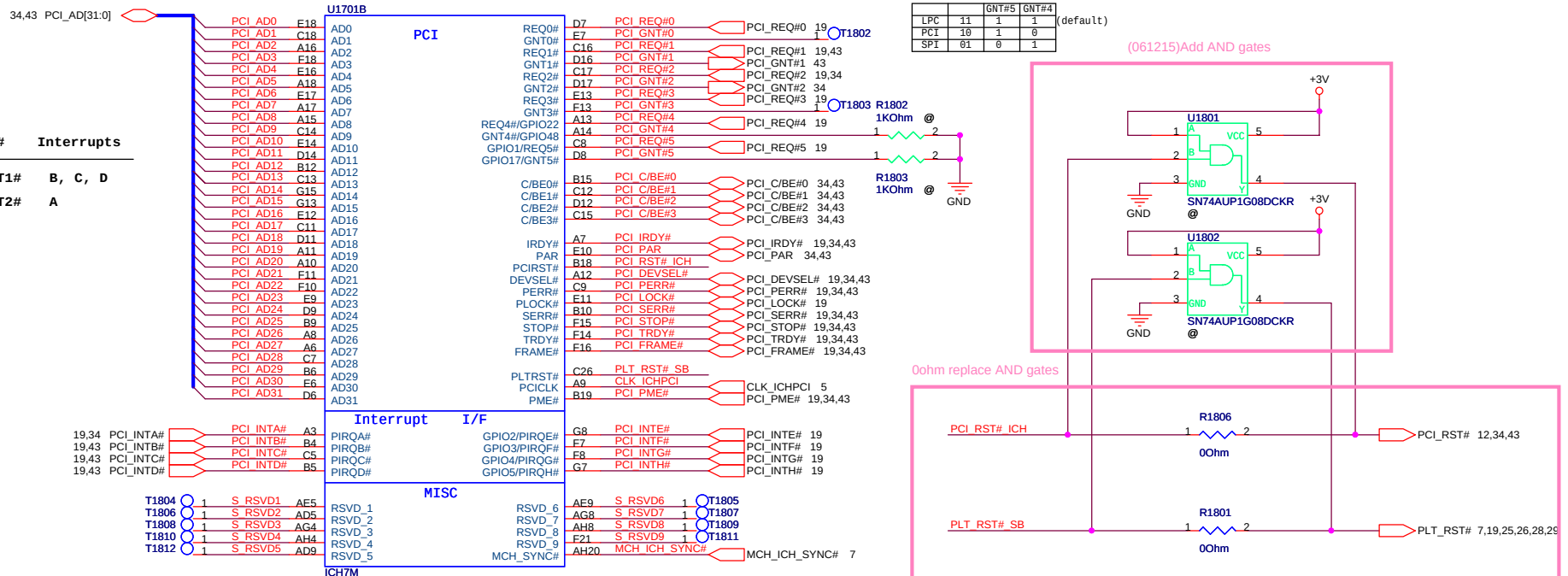
Check with EMI: remove 0 ohm
=>IDE_PDIOR#_ICH
IDE_PDD1_ICH
IDE_PDD2_ICH
IDE_PDD9_ICH
IDE_PDD10_ICH

ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

PCI Device

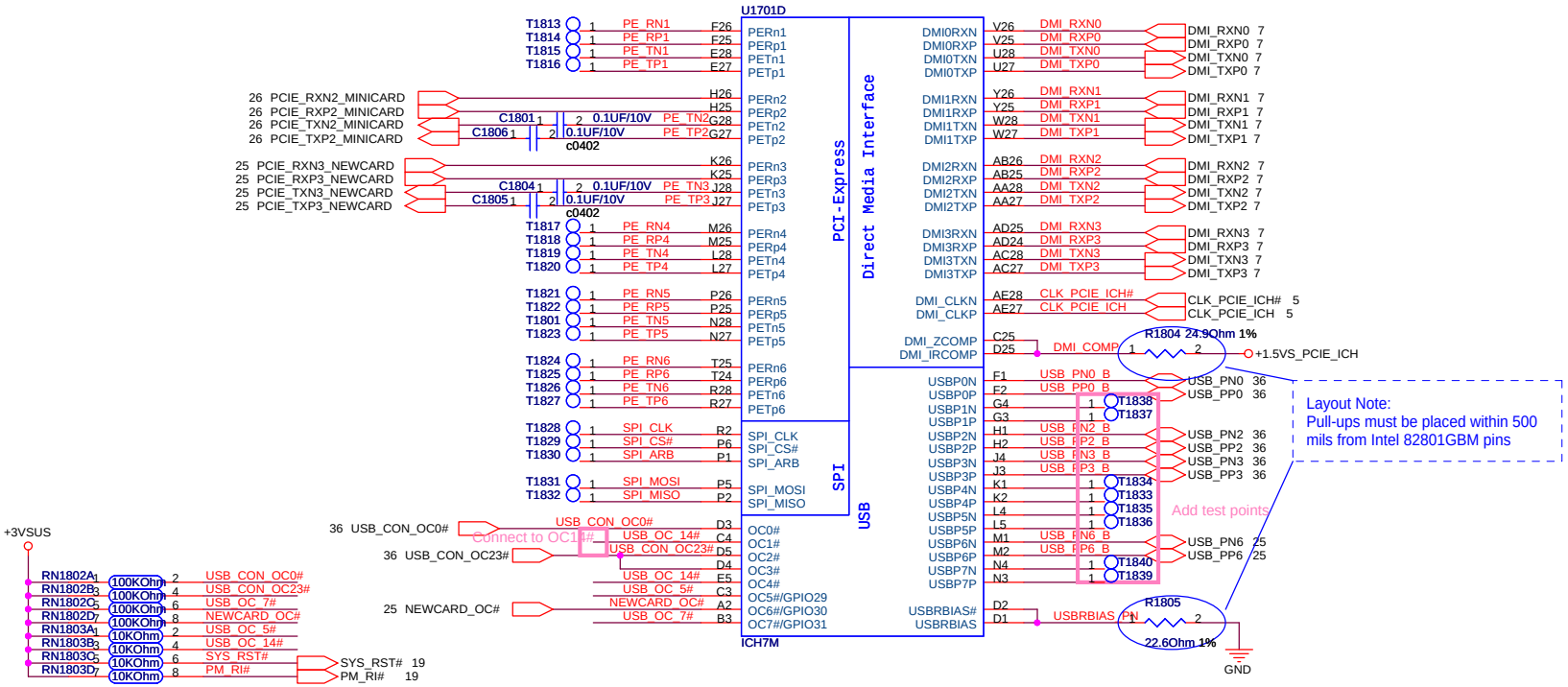
Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A



		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

(061215)Add AND gates

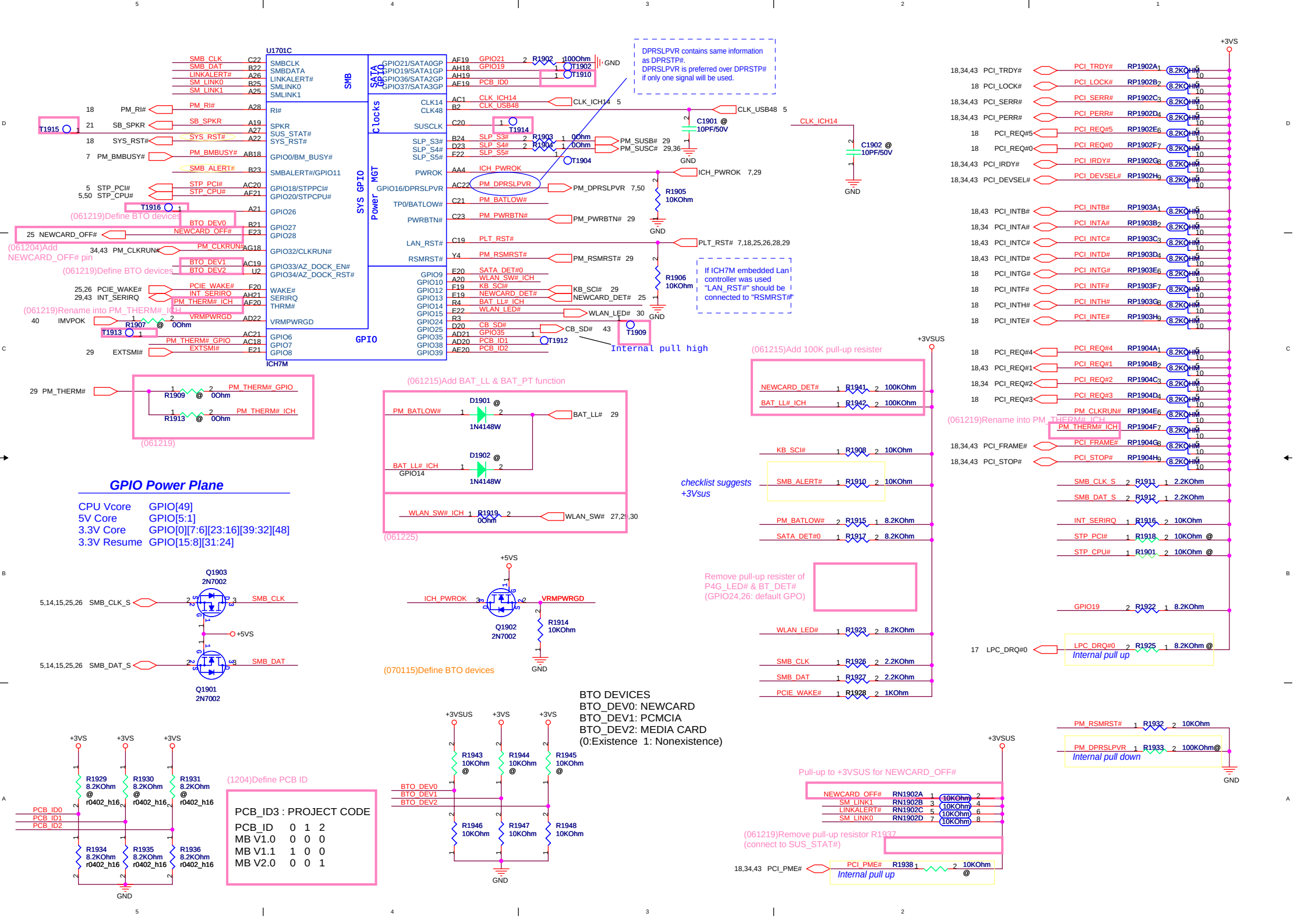
0ohm replace AND gates

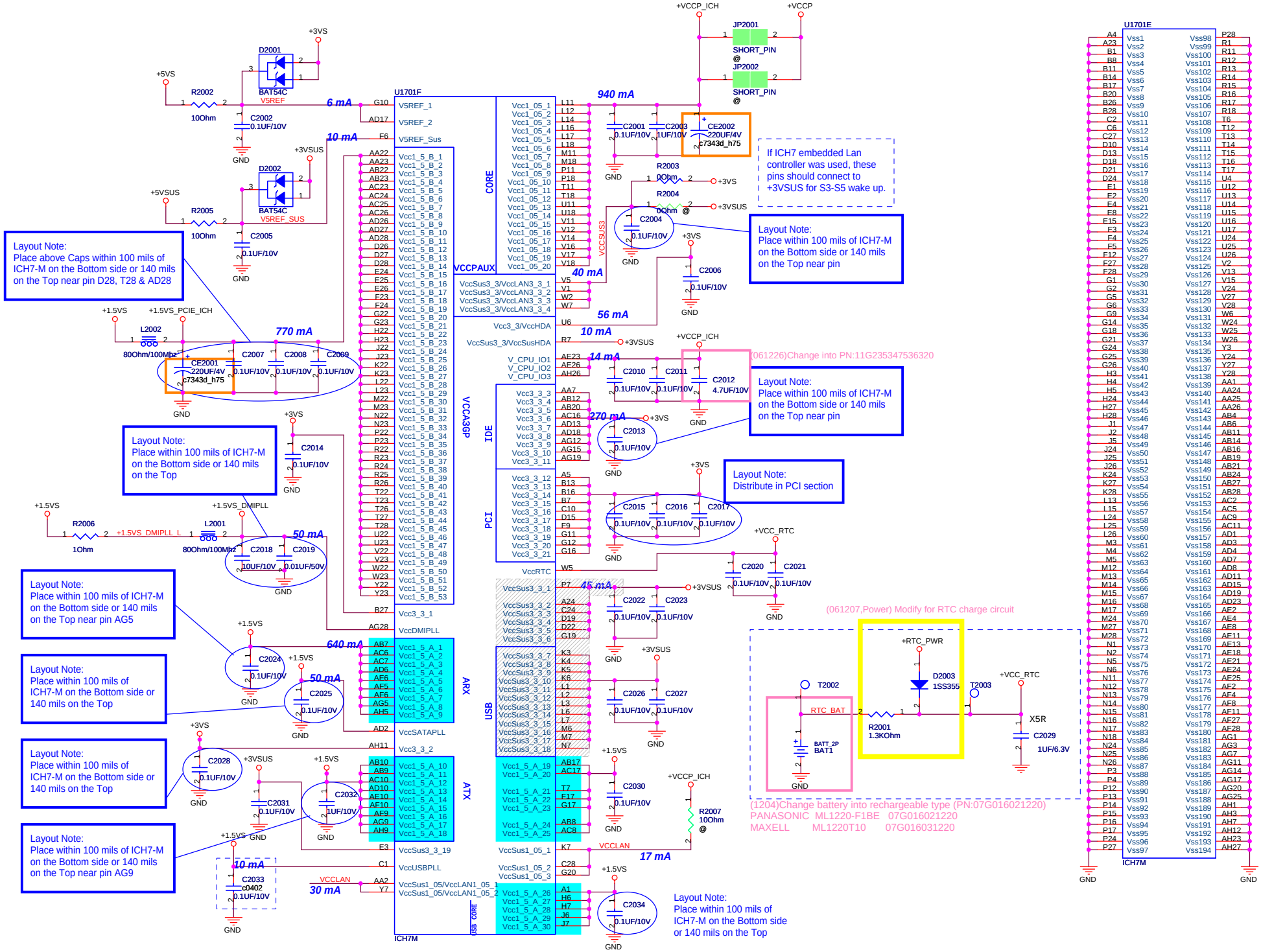


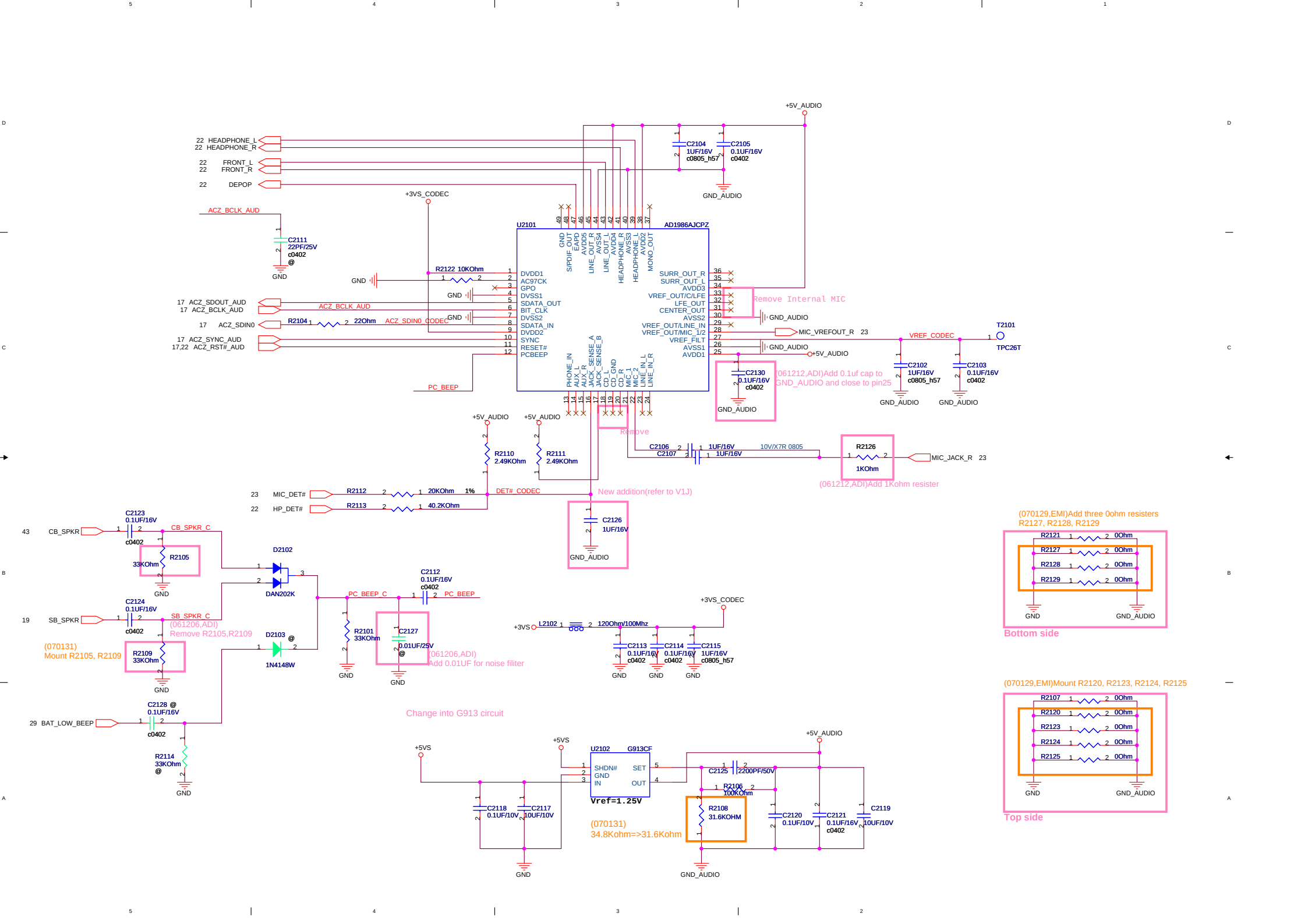
Modify USB Device table

USB Devices

Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	Unused


U1701C
ICH7M
SMB
SATA GP
Clocks
SYS GPIO
Power MGT
GPIO
SMB_CLK
SMB_DAT
LINKALERT#
SM_LINK0
SM_LINK1
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
PM_RI#
SB_SPKR
SYS_RST#
PM_BMBUSY#
SMB_ALERT#
STP_PCI#
STP_CPU#
BTO_DEV0
NEWCARD_OFF#
PM_CLKRUN#
BTO_DEV1
BTO_DEV2
PCIE_WAKE#
INT_SERIRQ
PM_THERM# ICH
VRMPWRGD
PM_THERM# GPIO
EXTSMI#
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
CLK_ICH14
CLK_USB48
ICH_PWROK
PM_DPRSLPVR
PM_BATLOW#
PM_PWRBTN#
PLT_RST#
PM_RSMRST#
SATA_DET#0
WLAN_SW# ICH
KB_SCI#
NEWCARD_DET#
BAT_LL# ICH
WLAN_LED#
CB_SD#
PCB_ID1
PCB_ID2
DPRSLPVR contains same information as DPRSTP#.
DPRSLPVR is preferred over DPRSTP# if only one signal will be used.
If ICH7M embedded Lan controller was used "LAN_RST#" should be connected to "RSMRST#"
Internal pull high
(061219)Define BTO devices
(061204)Add NEWCARD_OFF# pin
(061219)Rename into PM_THERM#_ICH
(061219)Add 100K pull-up resister
(061215)Add BAT_LL & BAT_PT function
(061225)
checklist suggests +3Vsus
Remove pull-up resister of P4G_LED# & BT_DET# (GPIO24,26: default GPO)
Internal pull up
Internal pull down
(070115)Define BTO devices
(1204)Define PCB ID
Pull-up to +3VSUS for NEWCARD_OFF#
(061219)Remove pull-up resistor R1937 (connect to SUS_STAT#)
GPIO Power Plane
CPU Vcore GPIO[49]
5V Core GPIO[5:1]
3.3V Core GPIO[0][7:6][23:16][39:32][48]
3.3V Resume GPIO[15:8][31:24]
BTO DEVICES
BTO_DEV0: NEWCARD
BTO_DEV1: PCMCIA
BTO_DEV2: MEDIA CARD
(0:Existence 1: Nonexistence)
PCB_ID3 : PROJECT CODE
PCB_ID 0 1 2
MB V1.0 0 0 0
MB V1.1 1 0 0
MB V2.0 0 0 1
Q1903 2N7002
Q1901 2N7002
Q1902 2N7002
D1901 1N4148W
D1902 1N4148W


U1701F
ICH7M
U1701E
ICH7M
CORE
VCCPAUX
VCCA3GP
IDE
PCI
USB
ATX
Layout Note:
Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Distribute in PCI section
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
(061226)Change into PN:11G235347536320
(061207,Power) Modify for RTC charge circuit
(1204)Change battery into rechargeable type (PN:07G016021220)
PANASONIC ML1220-F1BE 07G016021220
MAXELL ML1220T10 07G016031220
6 mA
10 mA
770 mA
940 mA
40 mA
56 mA
14 mA
270 mA
50 mA
640 mA
45 mA
17 mA
30 mA


22 HEADPHONE_L
22 HEADPHONE_R
22 FRONT_L
22 FRONT_R
22 DEPOP
+5V_AUDIO
C2104 1UF/16V c0805_h57
C2105 0.1UF/16V c0402
GND_AUDIO
+3VS_CODEC
ACZ_BCLK_AUD
C2111 22PF/25V c0402 @
GND
U2101
AD1986AJCPZ
R2122 10KOhm
17 ACZ_SDOUT_AUD
17 ACZ_BCLK_AUD
ACZ_BCLK_AUD
17 ACZ_SDIN0
R2104 22Ohm
ACZ_SDIN0_CODEC
17 ACZ_SYNC_AUD
17,22 ACZ_RST#_AUD
DVDD1
AC97CK
GPO
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET#
PCBEEP
SURR_OUT_R
SURR_OUT_L
AVDD3
VREF_OUT/C/LFE
LFE_OUT
CENTER_OUT
AVSS2
VREF_OUT/LINE_IN
VREF_OUT/MIC_1/2
VREF_FILT
AVSS1
AVDD1
Remove Internal MIC
MIC_VREFOUT_R 23
VREF_CODEC
T2101
TPC26T
C2130 0.1UF/16V c0402
(061212,ADI)Add 0.1uf cap to GND_AUDIO and close to pin25
C2102 1UF/16V c0805_h57
C2103 0.1UF/16V c0402
PC_BEEP
Remove
C2106 1UF/16V
C2107 1UF/16V
10V/X7R 0805
R2126 1KOhm
MIC_JACK_R 23
(061212,ADI)Add 1Kohm resister
R2110 2.49KOhm
R2111 2.49KOhm
23 MIC_DET#
R2112 20KOhm 1%
22 HP_DET#
R2113 40.2KOhm
DET#_CODEC
New addition(refer to V1J)
C2126 1UF/16V
43 CB_SPKR
C2123 0.1UF/16V c0402
CB_SPKR_C
R2105 33KOhm
D2102
DAN202K
19 SB_SPKR
C2124 0.1UF/16V c0402
SB_SPKR_C
(061206,ADI)
Remove R2105,R2109
(070131)
Mount R2105, R2109
R2109 33KOhm
D2103 @
1N4148W
PC_BEEP_C
C2112 0.1UF/16V c0402
PC_BEEP
R2101 33KOhm
C2127 0.01UF/25V @
(061206,ADI)
Add 0.01UF for noise filiter
+3VS
L2102 120Ohm/100Mhz
C2113 0.1UF/16V c0402
C2114 0.1UF/16V c0402
C2115 1UF/16V c0805_h57
29 BAT_LOW_BEEP
C2128 @ 0.1UF/16V c0402
R2114 33KOhm @
Change into G913 circuit
+5VS
U2102 G913CF
SHDN#
GND
IN
SET
OUT
Vref=1.25V
C2125 2200PF/50V
R2106 100KOhm
R2108 31.6KOHM
(070131)
34.8Kohm=>31.6Kohm
C2118 0.1UF/10V
C2117 10UF/10V
C2120 0.1UF/10V
C2121 0.1UF/16V c0402
C2119 10UF/10V
(070129,EMI)Add three 0ohm resisters
R2127, R2128, R2129
R2121 0Ohm
R2127 0Ohm
R2128 0Ohm
R2129 0Ohm
Bottom side
(070129,EMI)Mount R2120, R2123, R2124, R2125
R2107 0Ohm
R2120 0Ohm
R2123 0Ohm
R2124 0Ohm
R2125 0Ohm
Top side

(070126) Change R2201, R2202, R2203, R2204 into 27k ohm

R2202 27KOhm
C2202 68PF/50V
R2203 27KOhm
C2203 68PF/50V

21 FRONT_R
C2206 0.47UF/16V
R2206 10KOhm
R2209 10KOhm
C2208 1UF/10V
C2209 1UF/10V X7R

U2201
RLINEIN ROUT+ INTSPKR+
RHPIN ROUT- INTSPKR-
RBYPASS RVDD
MUTE IN TJ
MUTE OUT SE/BTL#
SHUTDOWN HP/LINE#
LBYPASS LVDD
NC1 NC2
LHPIN LOUT+ INTSPKL+
LLINEIN LOUT- INTSPKL-
GND/HS1 GND/HS2 THERMAL GND/HS3 GND/HS4
G1420F31UF

R2210 10KOhm
SE/BTL#

VDD_AMP
C2211 1UF/10V
C2213 0.1UF/16V
C2214 1UF/16V c0805_h57
C2215 1UF/16V c0805_h57
L2203 80Ohm/100Mhz
+5VS

GND_AUDIO

21 FRONT_L
C2216 1UF/10V
R2212 10KOhm
C2217 0.47UF/16V
R2214 10KOhm

C2218 68PF/50V
R2204 27KOhm
C2219 68PF/50V
R2201 27KOhm

(070110)modify JACK_IN circuit
JACK_IN
R2217 100KOhm
+3VS
21 HP_DET#
SE/BTL#
Q2201 2N7002
Q2202 2N7002
Q2207 2N7002

R2234 0Ohm @ INTSPKR+
R2235 0Ohm @ HEADPHONE_R 21

(061212,ADI) Placing Q2203, Q2205 on the other side of CE2202, CE2201
Q2203 2N7002
Q2205 2N7002
EAR_R
EAR_L
CE2202 330UF/6.3V
CE2201 330UF/6.3V
AOUTR_C
AOUTL_C
R2221 33Ohm
R2224 33Ohm
AJK_R
AJK_L
L2204 1KOhm/100Mhz
L2205 1KOhm/100Mhz
R2225 1KOhm
R2226 1KOhm

HP_JACK_R
HP_JACK_L
C2220 100PF/50V
C2221 100PF/50V
JACK_IN
L2201 1KOhm/100Mhz
C2223 100PF/50V

HP JACK
PHONE_JACK_6P
NP_NC2 NP_NC1 P_GND2 P_GND1
CON2202
GND_JACK

(070117)Change Phone Jack into PN:12G14000106M

100PF/50V use 11G2330101043 11---change

Change for Layout

(061213,ADI)GND_JACK connect to GND_AUDIO directly

+3VA +12VS +3VS
R2220 100KOhm
R2219 10MOhm
R2222 100KOhm r0402
R2223 100KOhm
C2222 0.47UF/16V c0603

17,21 ACZ_RST#_AUD
29 OP_SD#
D2201 BAT54AW
Q2208 2N7002
Q2204 2N7002
Q2206 2N7002
21 DEPOP

R2236 0Ohm HEADPHONE_L 21
R2237 @ 0Ohm INTSPKL+

(070130,EMI)Add 4 Varistors(D2202~D2205)
D2202 @ 0603-050E101NP-LF
D2203 @ 0603-050E101NP-LF
D2204 @ 0603-050E101NP-LF
D2205 @ 0603-050E101NP-LF

(070117) change into 12G17100004F
CON2203 SIDE2 SIDE1
WtoB_CON_4P

To Internal Speaker Connector
INTSPKL+ R2228 120Ohm/100Mhz
INTSPKL- R2229 120Ohm/100Mhz
INTSPKR+ R2231 120Ohm/100Mhz
INTSPKR- R2232 120Ohm/100Mhz

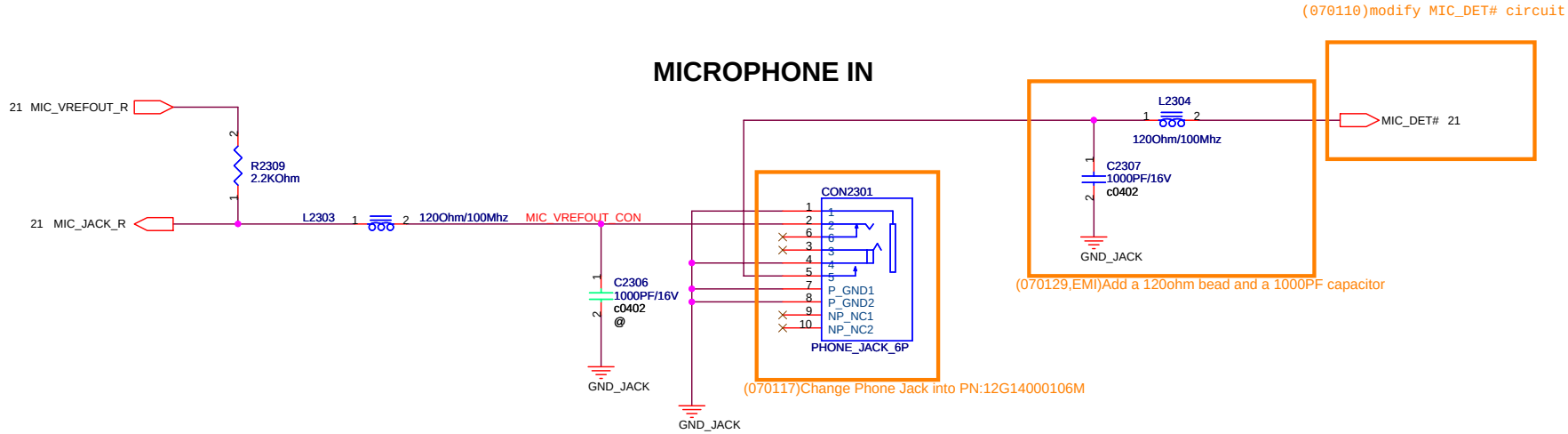
C2226 c0402 1000PF/50V
C2227 c0402 1000PF/50V
C2224 c0402 1000PF/50V
C2225 c0402 1000PF/50V

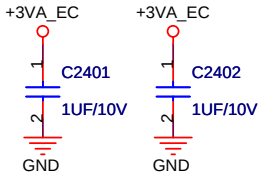
(061206,EMI) Add one 0ohm resister
R2240 0Ohm
R2233 0Ohm

(070129,EMI)Change 0ohm resisters into beads
L2238 120Ohm/100Mhz
L2239 120Ohm/100Mhz

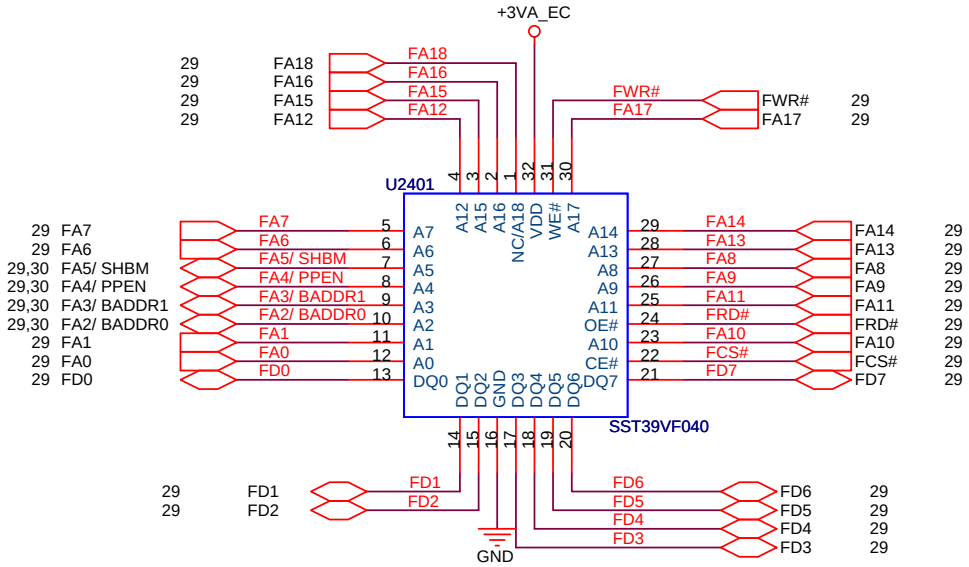
GND GND_AUDIO GND_JACK

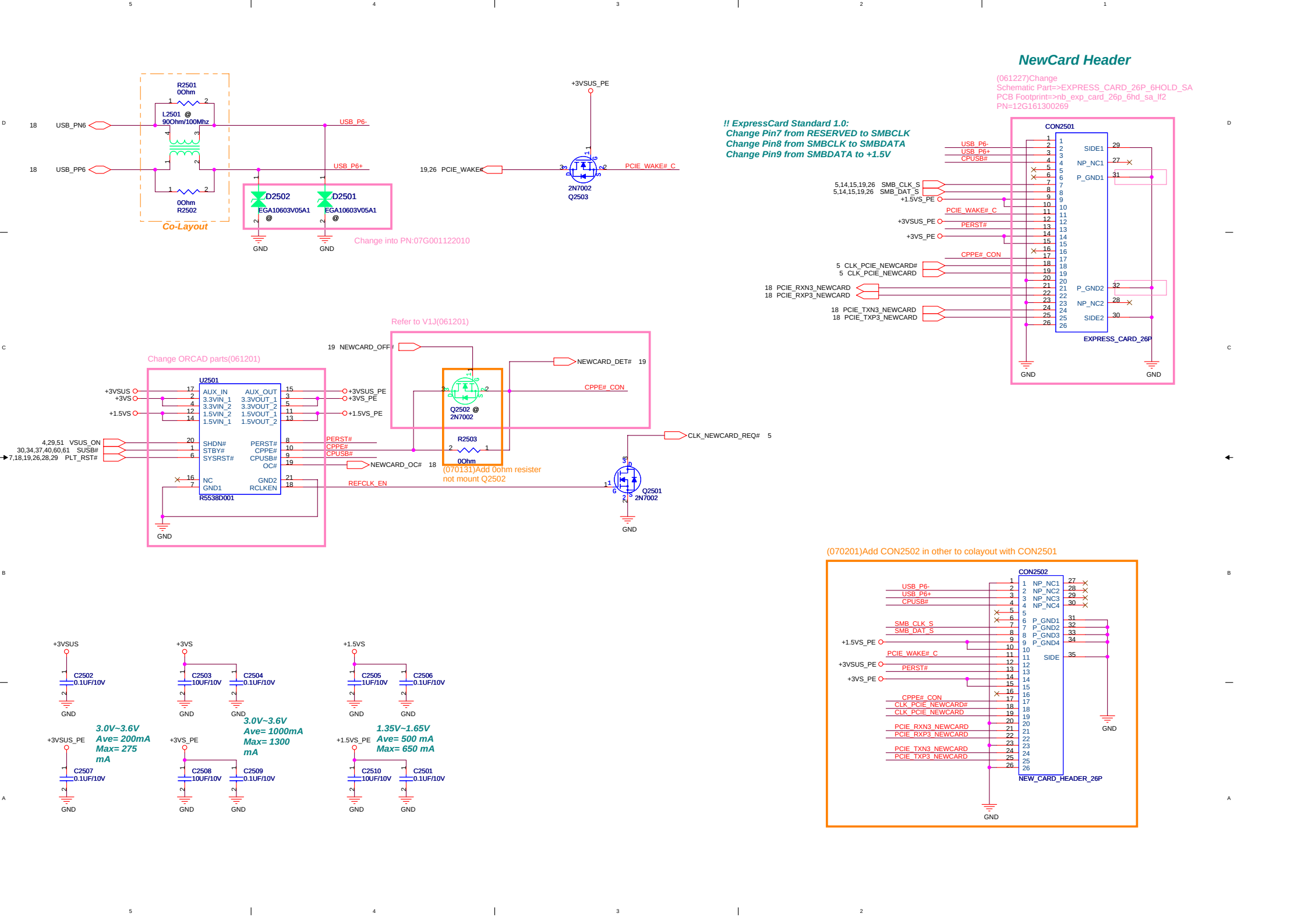
MICROPHONE IN




+3VA_EC
+3VA_EC
C2401
1UF/10V
C2402
1UF/10V
GND
GND

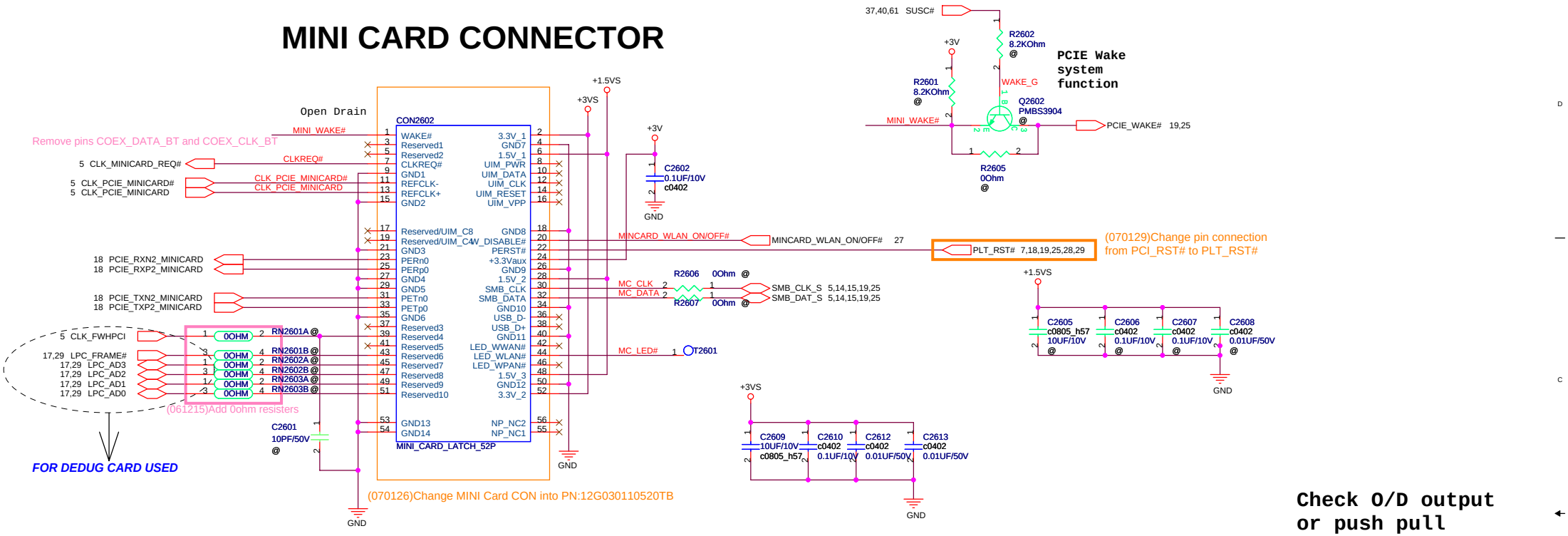
ISA ROM


+3VA_EC
U2401
SST39VF040
GND
FA18
FA16
FA15
FA12
FWR#
FA17
FA7
FA6
FA5/ SHBM
FA4/ PPEN
FA3/ BADDR1
FA2/ BADDR0
FA1
FA0
FD0
FA14
FA13
FA8
FA9
FA11
FRD#
FA10
FCS#
FD7
FD1
FD2
FD6
FD5
FD4
FD3


R2501
0Ohm
L2501 @
90Ohm/100Mhz
R2502
0Ohm
Co-Layout
18 USB_PN6
18 USB_PP6
USB_P6-
USB_P6+
D2502
EGA10603V05A1
@
D2501
EGA10603V05A1
@
GND
GND
Change into PN:07G001122010
+3VSUS_PE
19,26 PCIE_WAKE#
PCIE_WAKE#_C
2N7002
Q2503
NewCard Header
(061227)Change
Schematic Part=>EXPRESS_CARD_26P_6HOLD_SA
PCB Footprint=>nb_exp_card_26p_6hd_sa_lf2
PN=12G161300269
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V
CON2501
USB_P6-
USB_P6+
CPUSB#
5,14,15,19,26 SMB_CLK_S
5,14,15,19,26 SMB_DAT_S
+1.5VS_PE
PCIE_WAKE#_C
+3VSUS_PE
PERST#
+3VS_PE
CPPE#_CON
5 CLK_PCIE_NEWCARD#
5 CLK_PCIE_NEWCARD
18 PCIE_RXN3_NEWCARD
18 PCIE_RXP3_NEWCARD
18 PCIE_TXN3_NEWCARD
18 PCIE_TXP3_NEWCARD
SIDE1
NP_NC1
P_GND1
P_GND2
NP_NC2
SIDE2
EXPRESS_CARD_26P
GND
GND
Refer to V1J(061201)
Change ORCAD parts(061201)
19 NEWCARD_OFF#
NEWCARD_DET# 19
CPPE#_CON
Q2502 @
2N7002
R2503
0Ohm
CLK_NEWCARD_REQ# 5
(070131)Add 0ohm resister
not mount Q2502
U2501
+3VSUS
+3VS
+1.5VS
+3VSUS_PE
+3VS_PE
+1.5VS_PE
4,29,51 VSUS_ON
30,34,37,40,60,61 SUSB#
7,18,19,26,28,29 PLT_RST#
PERST#
CPPE#
CPUSB#
NEWCARD_OC# 18
REFCLK_EN
AUX_IN
AUX_OUT
3.3VIN_1
3.3VIN_2
1.5VIN_2
1.5VIN_1
3.3VOUT_1
3.3VOUT_2
1.5VOUT_1
1.5VOUT_2
SHDN#
STBY#
SYSRST#
PERST#
CPPE#
CPUSB#
OC#
NC
GND1
GND2
RCLKEN
R5538D001
Q2501
2N7002
GND
GND
(070201)Add CON2502 in other to colayout with CON2501
CON2502
USB_P6-
USB_P6+
CPUSB#
SMB_CLK_S
SMB_DAT_S
+1.5VS_PE
PCIE_WAKE#_C
+3VSUS_PE
PERST#
+3VS_PE
CPPE#_CON
CLK_PCIE_NEWCARD#
CLK_PCIE_NEWCARD
PCIE_RXN3_NEWCARD
PCIE_RXP3_NEWCARD
PCIE_TXN3_NEWCARD
PCIE_TXP3_NEWCARD
NP_NC1
NP_NC2
NP_NC3
NP_NC4
P_GND1
P_GND2
P_GND3
P_GND4
SIDE
NEW_CARD_HEADER_26P
GND
GND
+3VSUS
C2502
0.1UF/10V
GND
+3VS
C2503
10UF/10V
C2504
0.1UF/10V
GND
GND
3.0V~3.6V
Ave= 1000mA
Max= 1300
mA
+1.5VS
C2505
1UF/10V
C2506
0.1UF/10V
GND
GND
1.35V~1.65V
Ave= 500 mA
Max= 650 mA
+3VSUS_PE
C2507
0.1UF/10V
GND
3.0V~3.6V
Ave= 200mA
Max= 275
mA
+3VS_PE
C2508
10UF/10V
C2509
0.1UF/10V
GND
GND
+1.5VS_PE
C2510
10UF/10V
C2501
0.1UF/10V
GND
GND

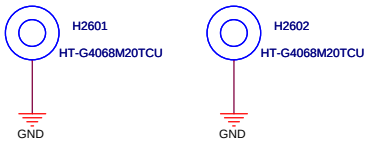
(061212) Not mount (Not support wake on WLAN)

MINI CARD CONNECTOR



Check O/D output or push pull

Instead of Mini-PCIE latch connecter.For cost down.



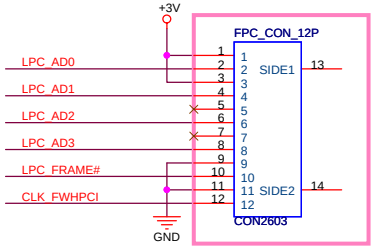
(070201)Change MINI Card NUT into PN:13G021056061TB

WLAN SPEC:

		WLL3140	WLL4080
Transmit Mode Current	11.a		550mA
	11.b	525mA	560mA
	11.g	560mA	550mA
	11.n		
Receive Mode Current	11.a		280mA
	11.b	430mA	270mA
	11.g	460mA	280mA
	11.n		
Sleep Mode Current		220mA	20mA
Supplied Voltage(VCC)	MIN	3.0V	3.0V
	TYP	3.3V	3.3V
	MAX	3.6V	3.6V

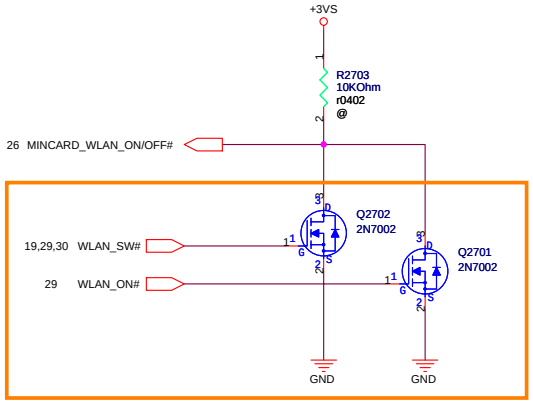
Debug Card CON

(061206)Change Debug CON into PN:12G18340120E



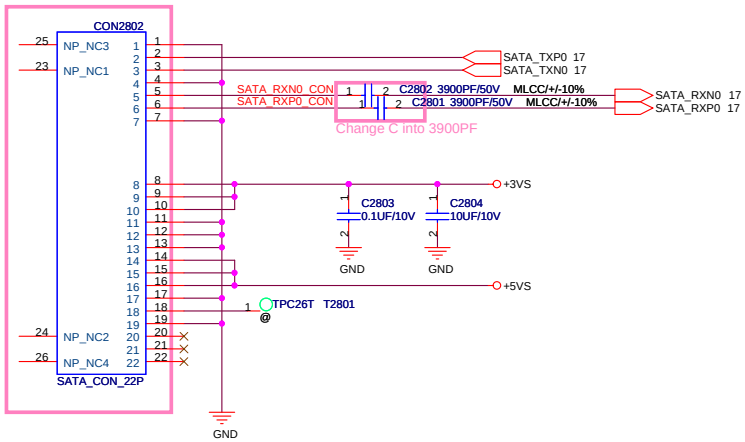
For Side SW

WLAN ON/OFF Control

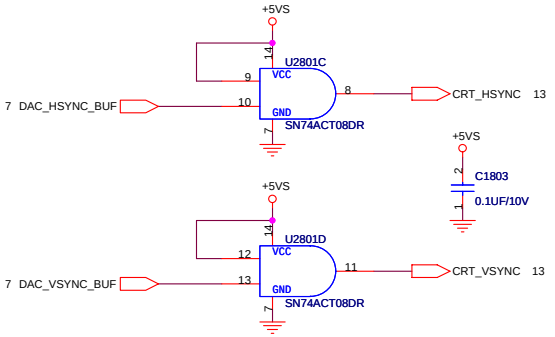


(070202)Modify WLAN on/off circuit

(061208)Change SATA CON into PN:12G15101022A

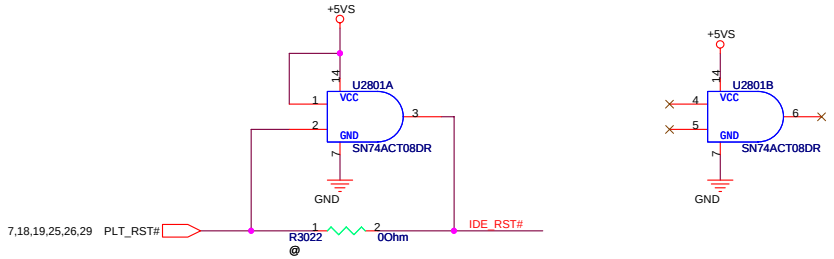


Change AND gate into 5V Vcc

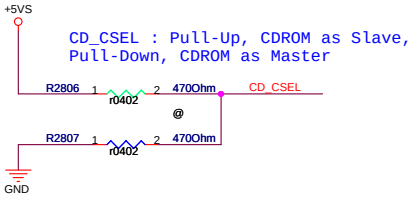


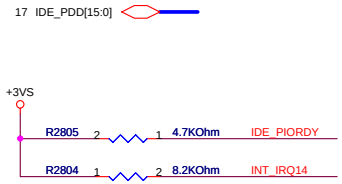
SATA HDD

Modify



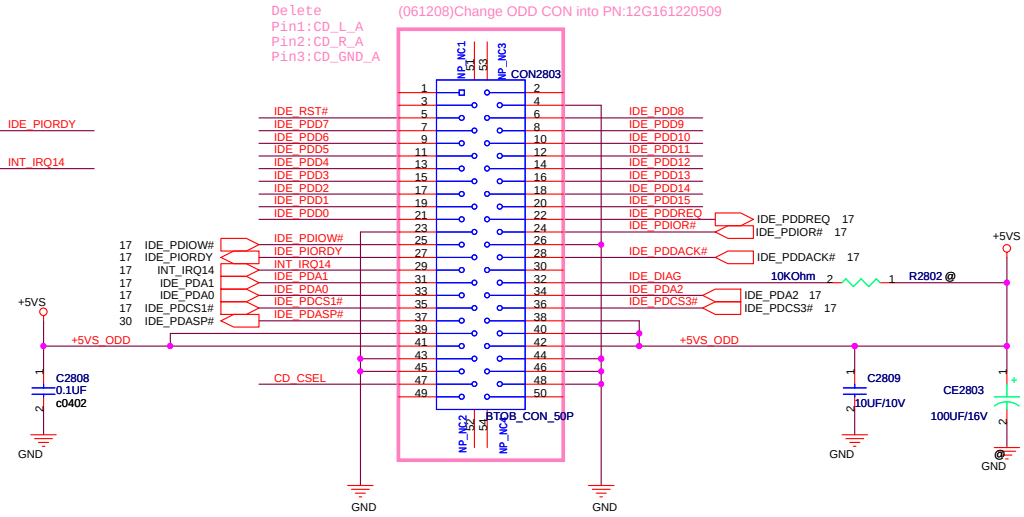
CD-ROM





Delete
Pin1:CD_L_A
Pin2:CD_R_A
Pin3:CD_GND_A

(061208)Change ODD CON into PN:12G161220509



TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

U2901 IT8511E

(061222)Remove netname
pin 1
pin 47
pin 171

close to EC

Cload=12.5PF

(061215)Add CHG_FULL_LED#_EC pin

Delete pull-up resisters:
DJ_SW#, BT_ON#

(061214)Remove PWRLMT#

Remove MARATHON# & DISTP#,
but need to be pulled up

(061222)Change pin48,148 netname

watchdog

(061219)New addition

(061215)Add ID pin

(061222)Add pin86 netname

Add test point

Follow Z94 Keyboard

Option1:
Mount R2926, R2918, C2917, D2904
Not mount C2910, C2912, U2902
Option 2:
Mount C2910, C2912, U2902
Not mount R2926, R2918, C2917, D2904

(070131)change into 1%

(070131)change into 10%

Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms

(070202)Connect to +3VSUS

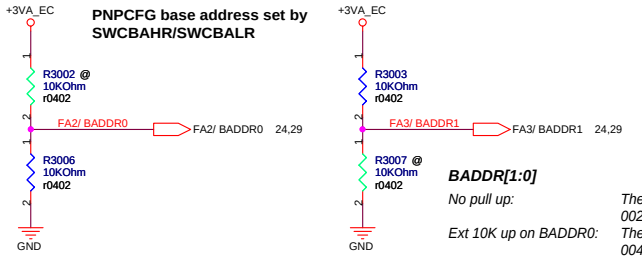
(0611222)
Modify into input port

(0611213)Keyboard pin definition is the same as F3 series
PN=12G182402806

Layout Note:
Close to Switch

EC Hardware Strap

Strap value sampled after VSTBY power up reset

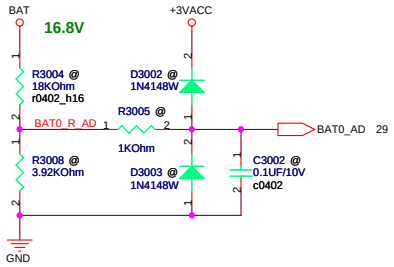


BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

EC ADC

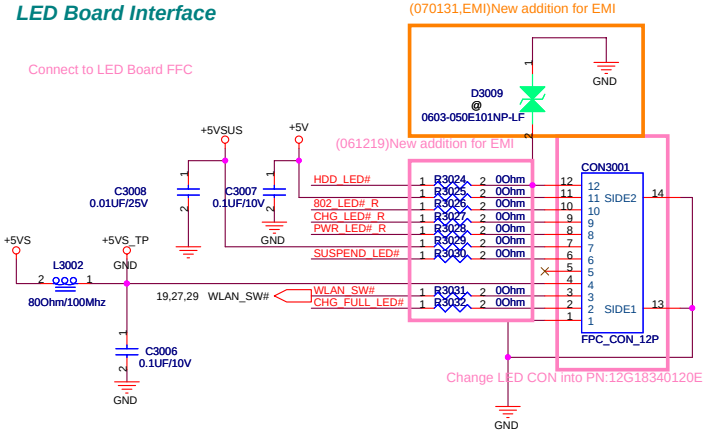
Battery



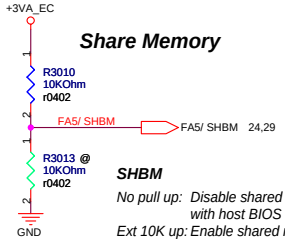
LED Board Interface

(070131,EMI)New addition for EMI

Connect to LED Board FFC

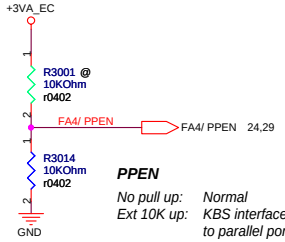


Share Memory



SHBM

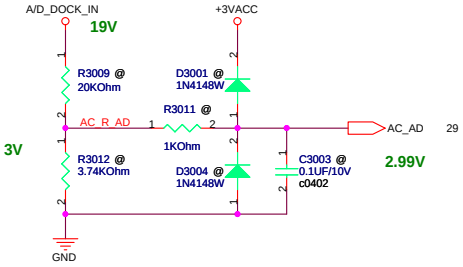
No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*



PPEN

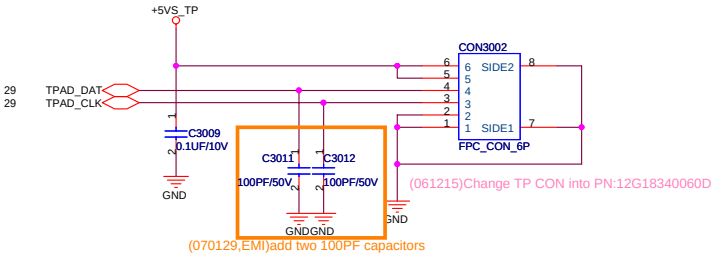
No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

Adaptor

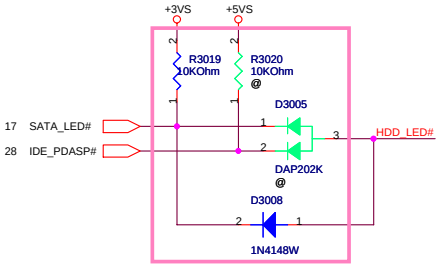


Touchpad Board Interface

Connect to Touchpad Board FFC



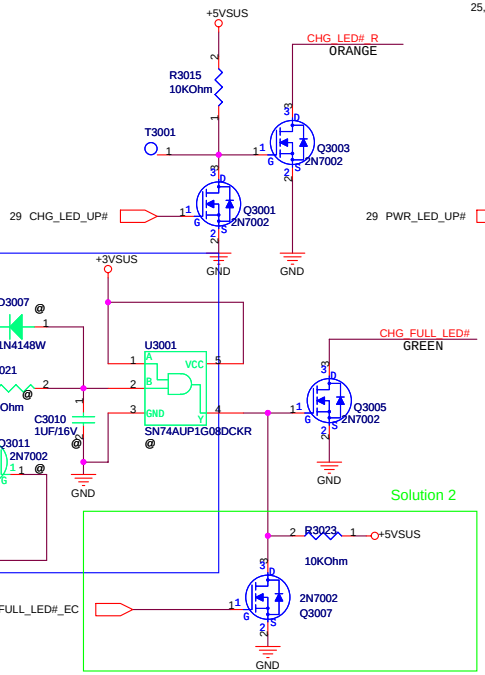
HDD LED



(061212)Modify HDD LED circuit

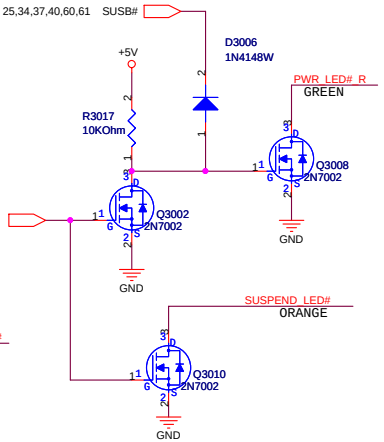
(061201)Modify Charge & Power circuit

CHARGE LED

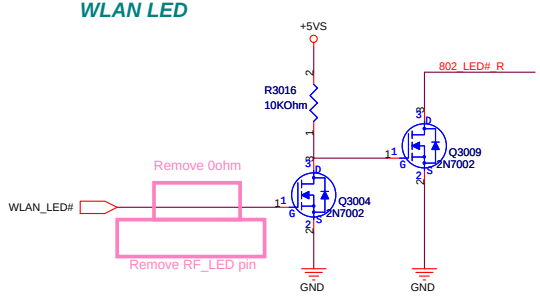


(061212)Modify charge full circuit : solution1 & solution2

POWER LED



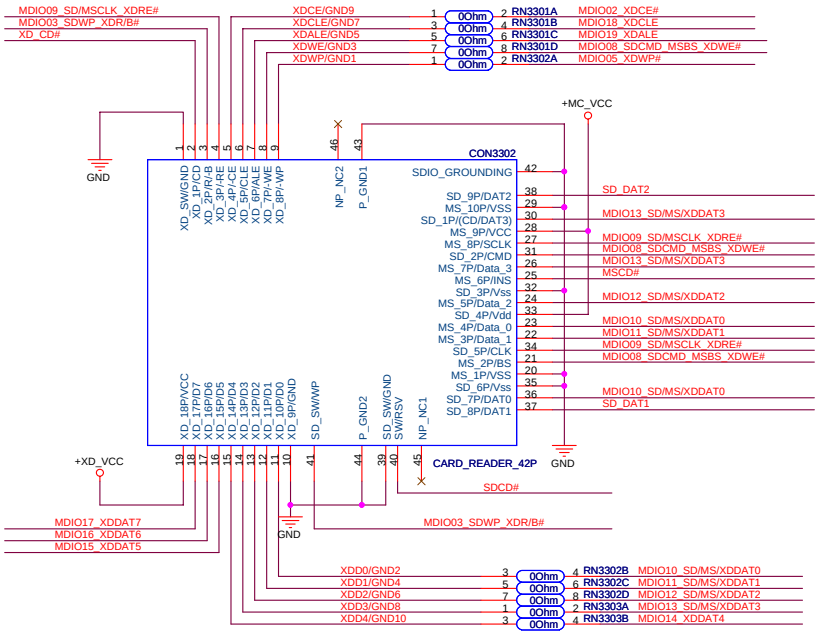
WLAN LED



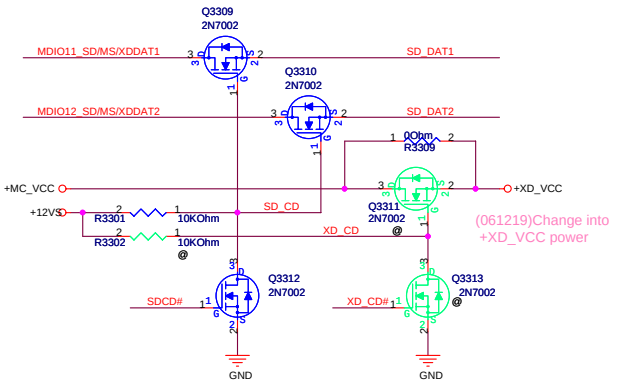
MEDIA CARD SLOT

(070124)Add Media Card CON for colayout

(070130)Add RN3301, RN3302, RN3303



Solve-MS Duo Adaptor short problem / XD short problem

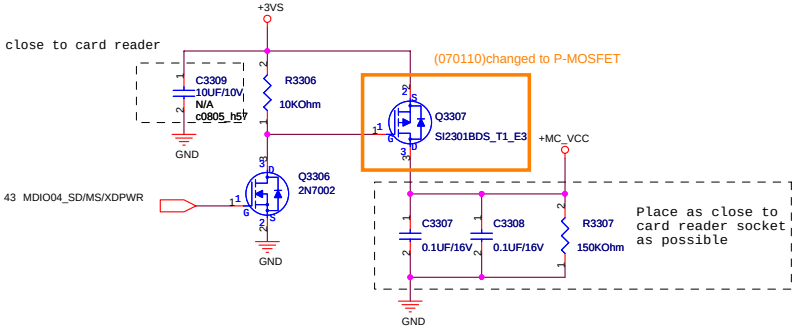


(061219)Change into +XD_VCC power

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

Change circuit from AAT4610A to SI2301

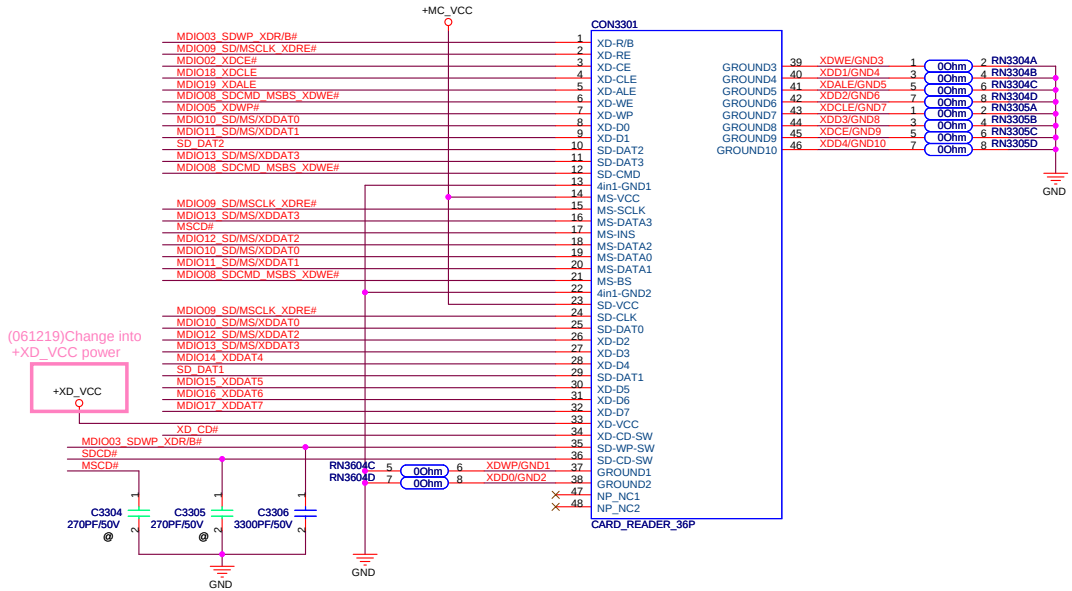
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low



MEDIA CARD SLOT

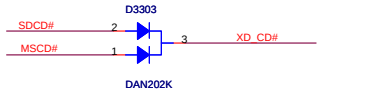
(061208)Change CON3301 into PN:12G340003601
(061225)Change schematic part & PCB Footprint

(070130)Add RN3303, RN3304, RN3305

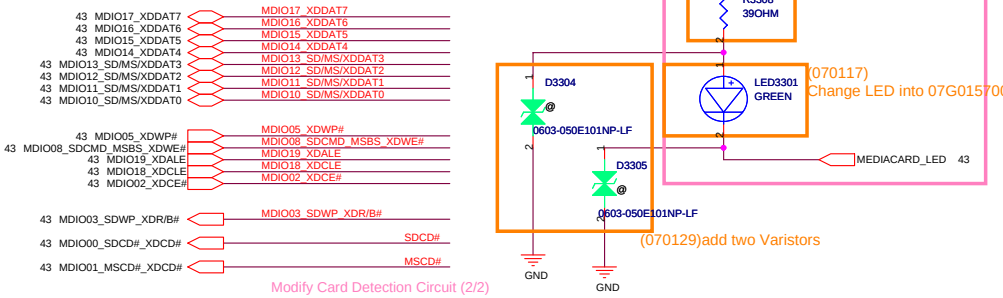


(061219)Change into +XD_VCC power

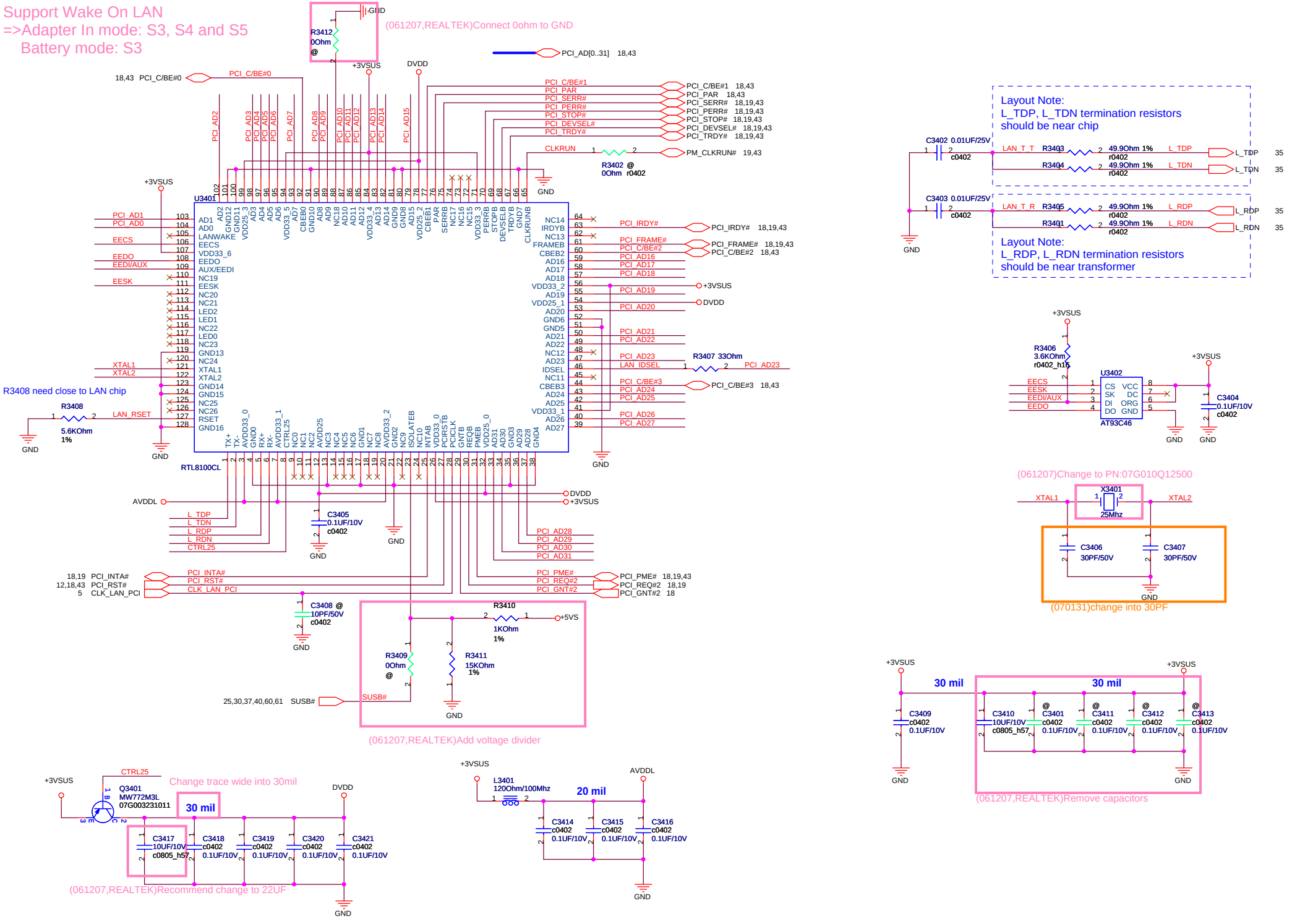
Modify Card Detection Circuit (1/2)



(161219)Change reference into R3308&LED3301



Support Wake On LAN
=>Adapter In mode: S3, S4 and S5
Battery mode: S3



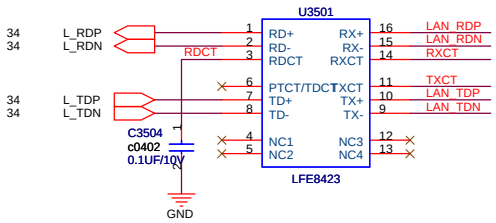
(061207)Change to PN:07G010Q12500

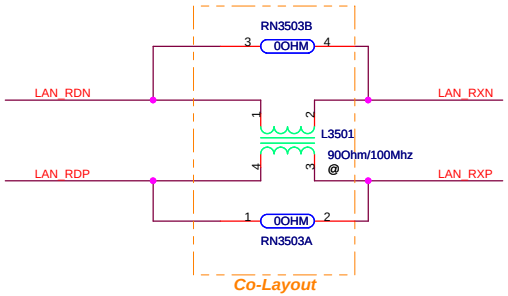
(070131)change into 30PF

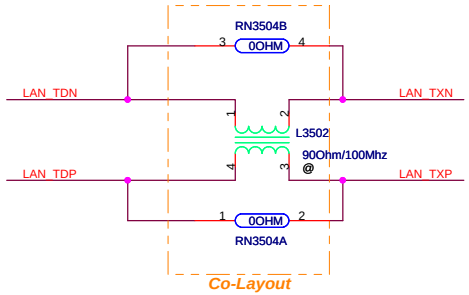
(061207,REALTEK)Remove capacitors

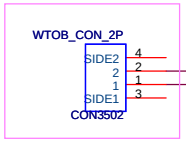
LAN PORT

TRANSFORMER 10/100MB



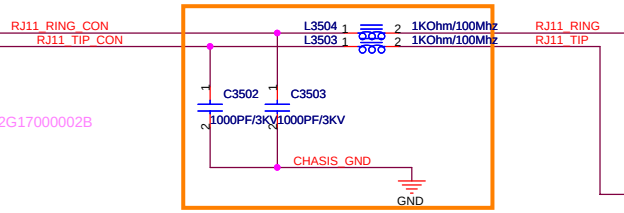




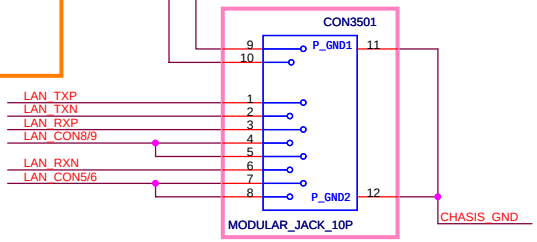


(061214)Change CON3502 into PN:12G17000002B

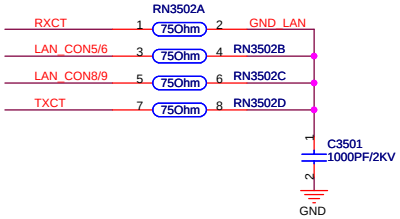
(070131)place C3502, C3503 on the other side of L3503, L3504



RJ11&RJ45



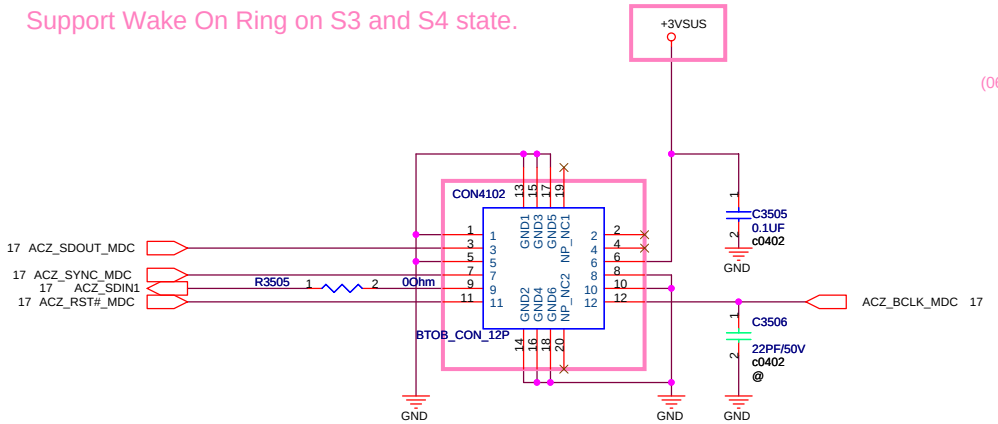
(061214)Change RJ11&RJ45 into PN:12G142011109



MDC CONNECTOR

Support Wake On Ring on S3 and S4 state.

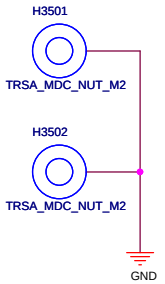
Change power from +3V to +3VSUS

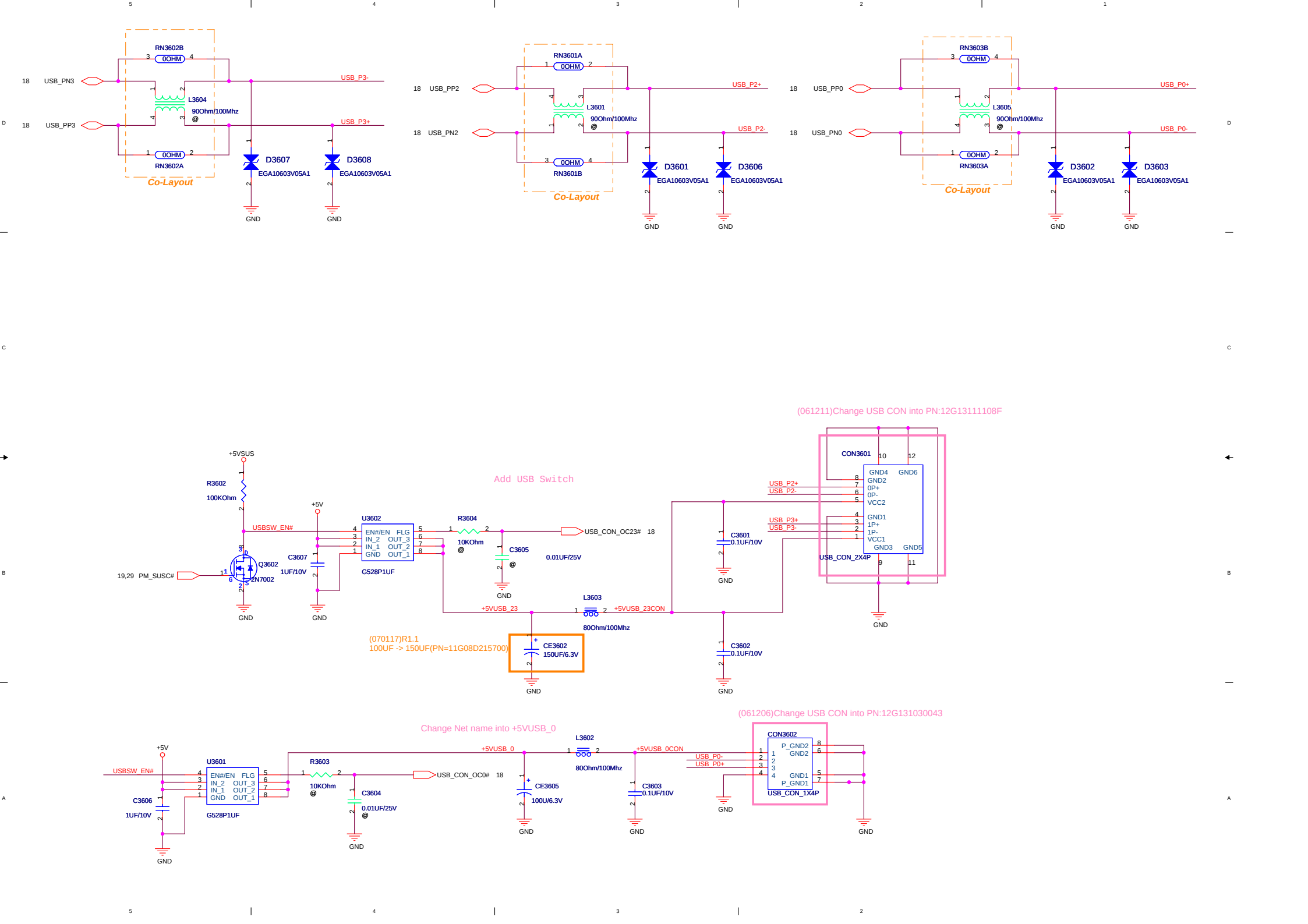


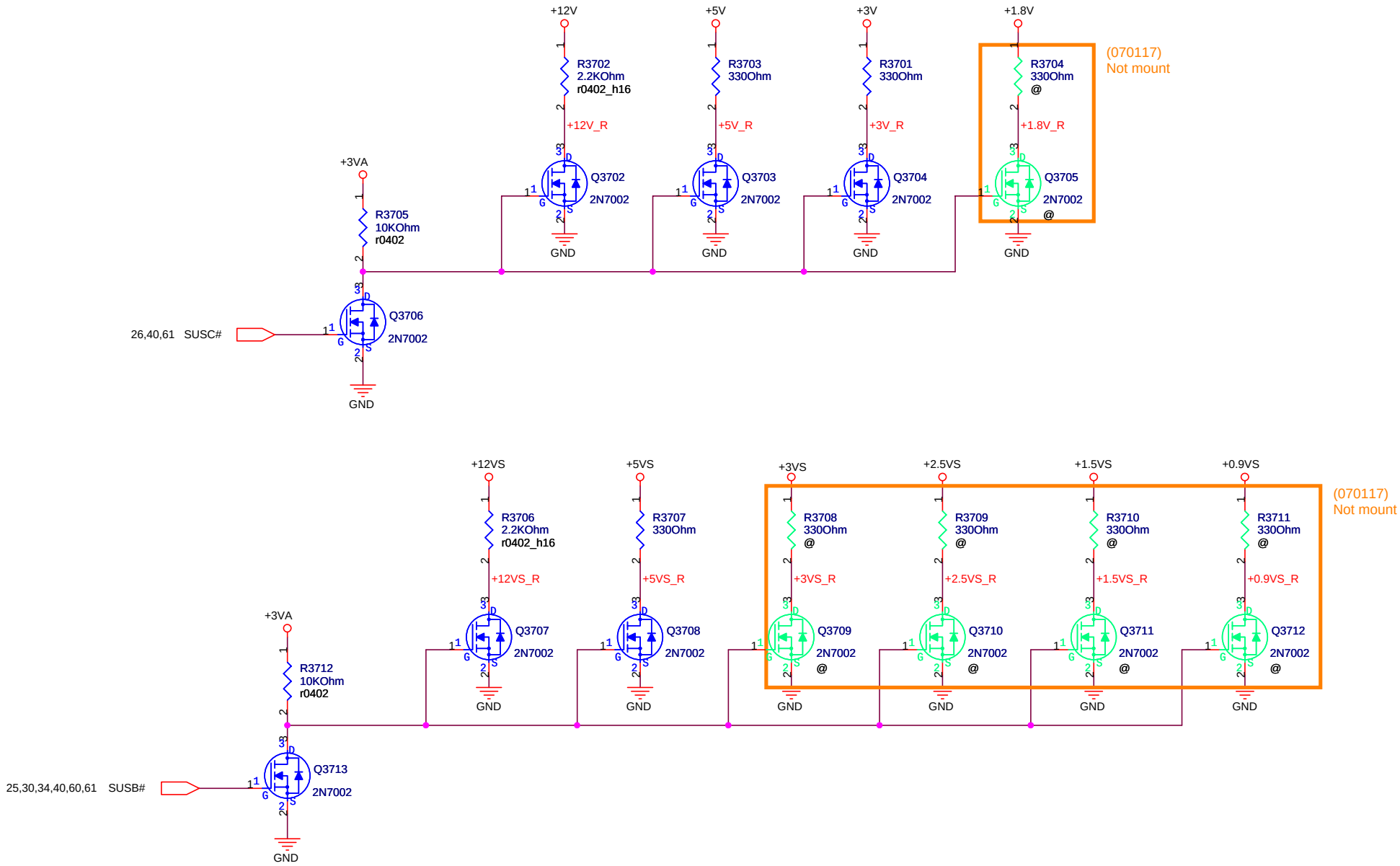
(061214)Change MDC CON into PN:12G16020012D

B:MDC NUT

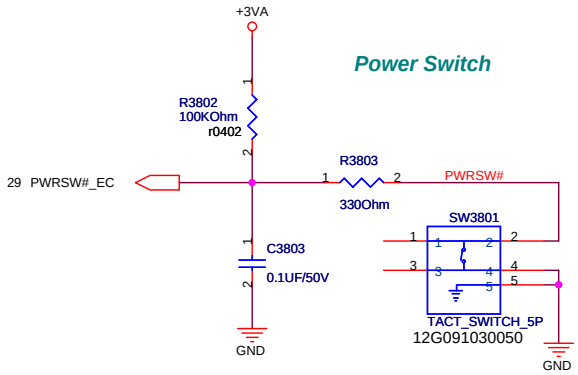
(061219)Change MDC NUT into PN:13G021054000

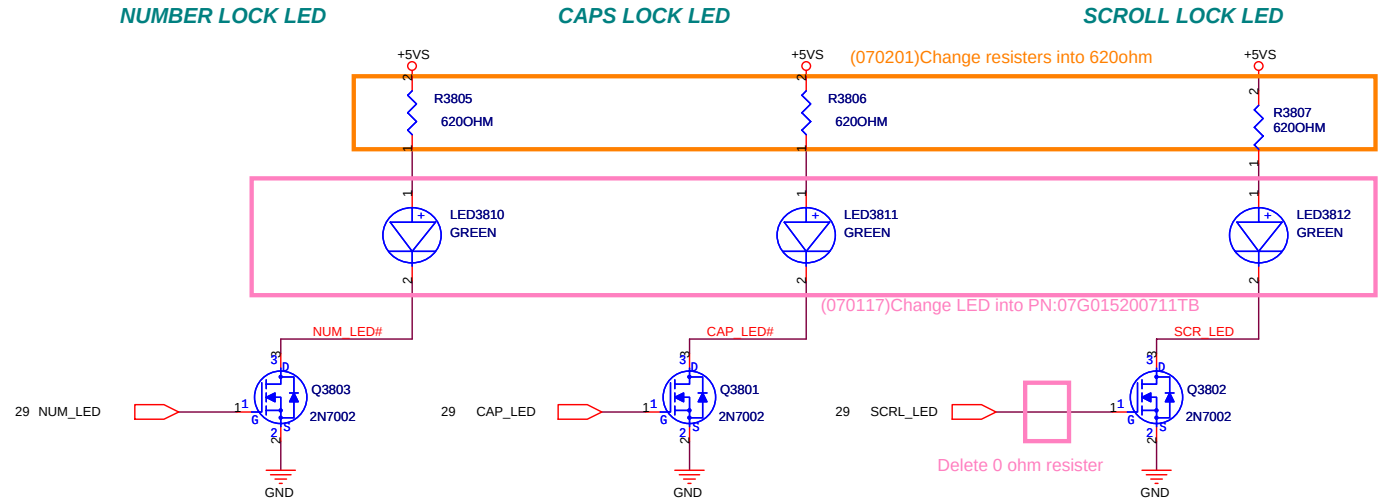


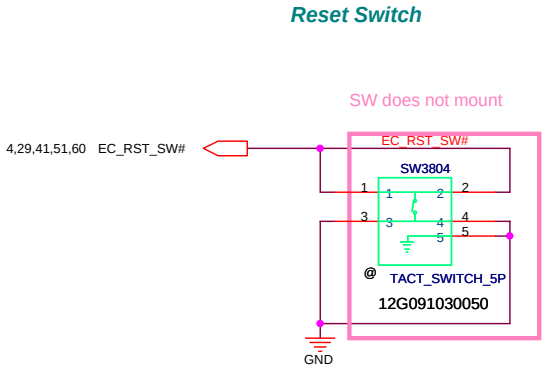

RN3602B
0OHM
L3604
90Ohm/100Mhz
@
RN3602A
0OHM
D3607
EGA10603V05A1
D3608
EGA10603V05A1
GND
Co-Layout
18 USB_PN3
18 USB_PP3
USB_P3-
USB_P3+
RN3601A
0OHM
L3601
90Ohm/100Mhz
@
RN3601B
0OHM
D3601
EGA10603V05A1
D3606
EGA10603V05A1
Co-Layout
18 USB_PP2
18 USB_PN2
USB_P2+
USB_P2-
RN3603B
0OHM
L3605
90Ohm/100Mhz
@
RN3603A
0OHM
D3602
EGA10603V05A1
D3603
EGA10603V05A1
Co-Layout
18 USB_PP0
18 USB_PN0
USB_P0+
USB_P0-
(061211)Change USB CON into PN:12G13111108F
Add USB Switch
+5VSUS
R3602
100KOhm
USBSW_EN#
19,29 PM_SUSC#
Q3602
2N7002
+5V
C3607
1UF/10V
U3602
EN#/EN FLG
IN_2 OUT_3
IN_1 OUT_2
GND OUT_1
G528P1UF
R3604
10KOhm
@
C3605
0.01UF/25V
USB_CON_OC23# 18
+5VUSB_23
L3603
80Ohm/100Mhz
+5VUSB_23CON
(070117)R1.1
100UF -> 150UF(PN=11G08D215700)
CE3602
150UF/6.3V
C3601
0.1UF/10V
C3602
0.1UF/10V
CON3601
GND4 GND6
GND2
0P+
0P-
VCC2
GND1
1P+
1P-
VCC1
GND3 GND5
USB_CON_2X4P
USB_P2+
USB_P2-
USB_P3+
USB_P3-
Change Net name into +5VUSB_0
(061206)Change USB CON into PN:12G131030043
+5V
USBSW_EN#
U3601
EN#/EN FLG
IN_2 OUT_3
IN_1 OUT_2
GND OUT_1
G528P1UF
C3606
1UF/10V
R3603
10KOhm
@
C3604
0.01UF/25V
@
USB_CON_OC0# 18
+5VUSB_0
L3602
80Ohm/100Mhz
+5VUSB_0CON
CE3605
100U/6.3V
C3603
0.1UF/10V
CON3602
P_GND2
GND2
GND1
P_GND1
USB_CON_1X4P
USB_P0-
USB_P0+

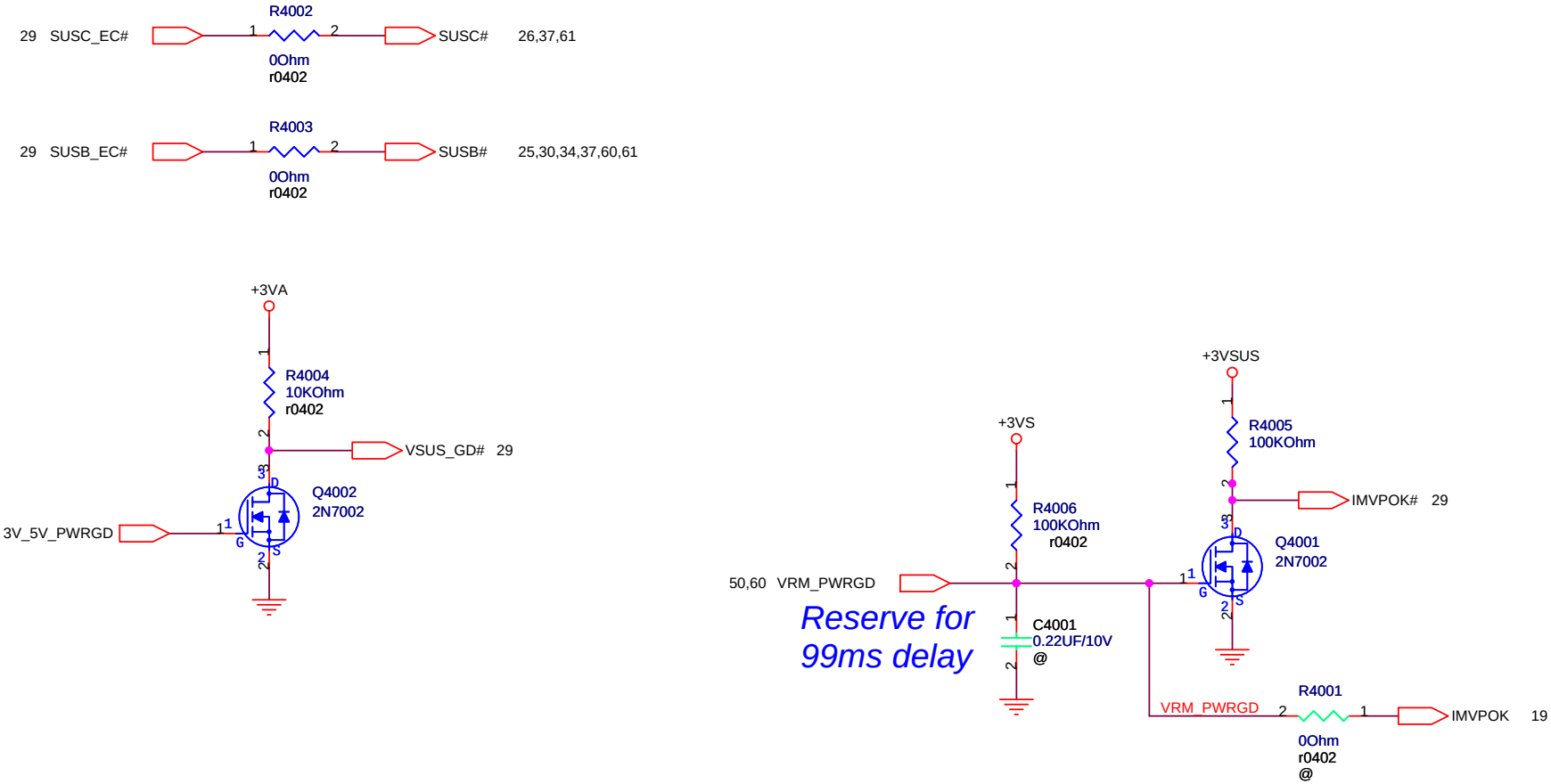

+12V
+5V
+3V
+1.8V
R3702
2.2KOhm
r0402_h16
R3703
330Ohm
R3701
330Ohm
R3704
330Ohm
@
(070117)
Not mount
+12V_R
+5V_R
+3V_R
+1.8V_R
Q3702
Q3703
Q3704
Q3705
2N7002
@
GND
+3VA
R3705
10KOhm
r0402
Q3706
2N7002
26,40,61 SUSC#
+12VS
+5VS
+3VS
+2.5VS
+1.5VS
+0.9VS
R3706
2.2KOhm
r0402_h16
R3707
330Ohm
R3708
330Ohm
@
R3709
330Ohm
@
R3710
330Ohm
@
R3711
330Ohm
@
(070117)
Not mount
+12VS_R
+5VS_R
+3VS_R
+2.5VS_R
+1.5VS_R
+0.9VS_R
Q3707
Q3708
Q3709
Q3710
Q3711
Q3712
2N7002
@
+3VA
R3712
10KOhm
r0402
Q3713
2N7002
25,30,34,40,60,61 SUSB#
GND

Main Board SW & LED

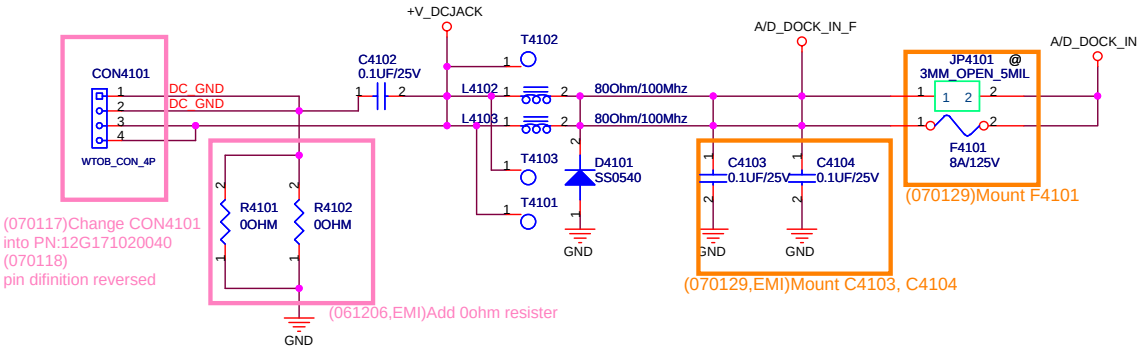




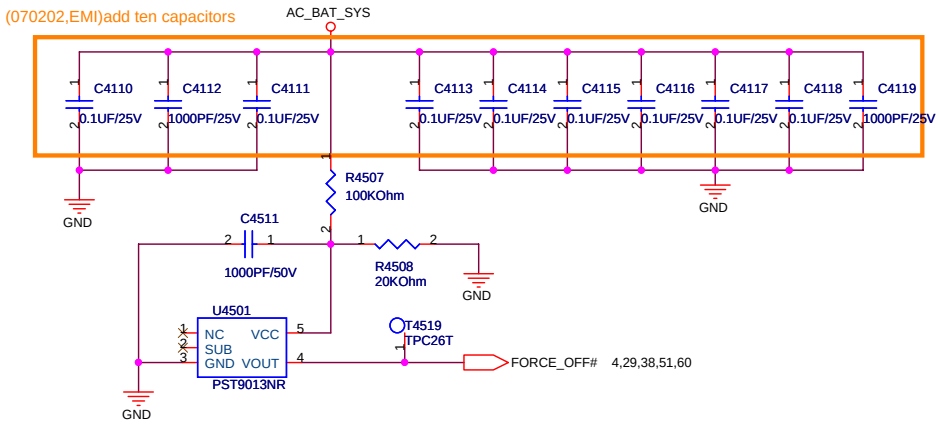


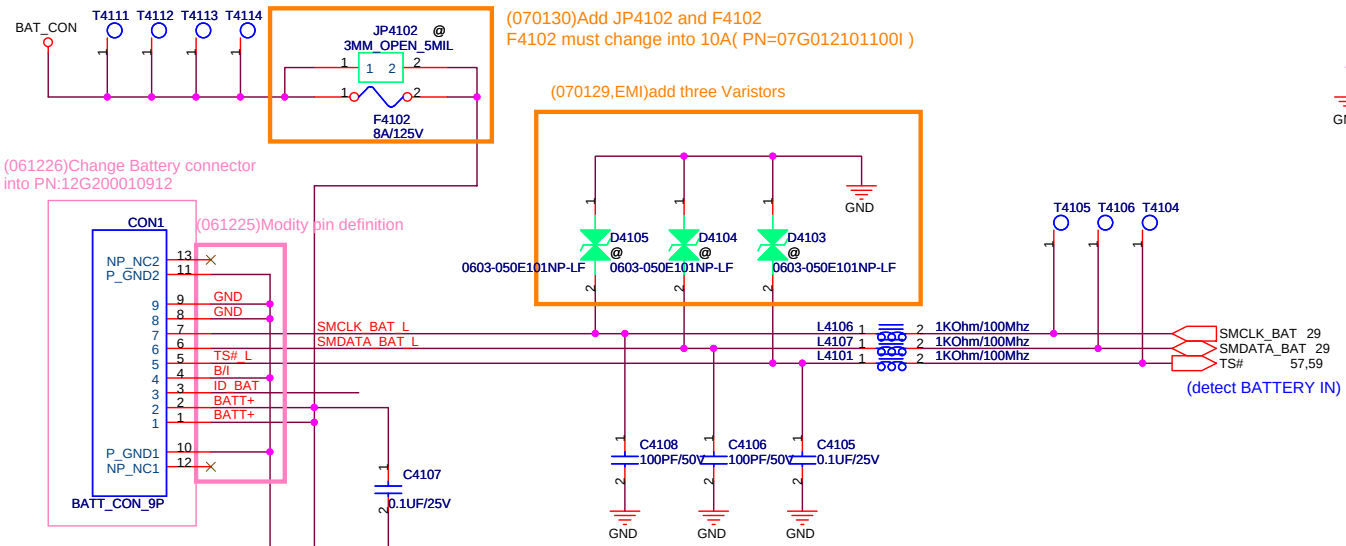

R4002
29 SUSC_EC#
1
2
SUSC#
26,37,61
0Ohm
r0402
R4003
29 SUSB_EC#
1
2
SUSB#
25,30,34,37,60,61
0Ohm
r0402
+3VA
R4004
10KOhm
r0402
VSUS_GD# 29
Q4002
2N7002
51,60 3V_5V_PWRGD
+3VSUS
+3VS
R4005
100KOhm
R4006
100KOhm
r0402
IMVPOK# 29
Q4001
2N7002
50,60 VRM_PWRGD
Reserve for
99ms delay
C4001
0.22UF/10V
@
VRM_PWRGD
R4001
IMVPOK 19
0Ohm
r0402
@

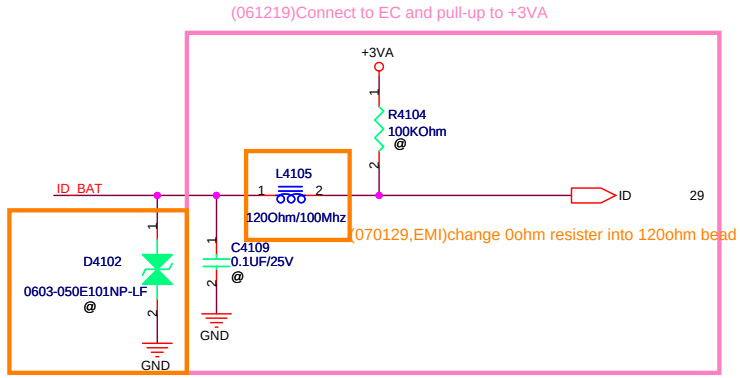
DC Power Jack

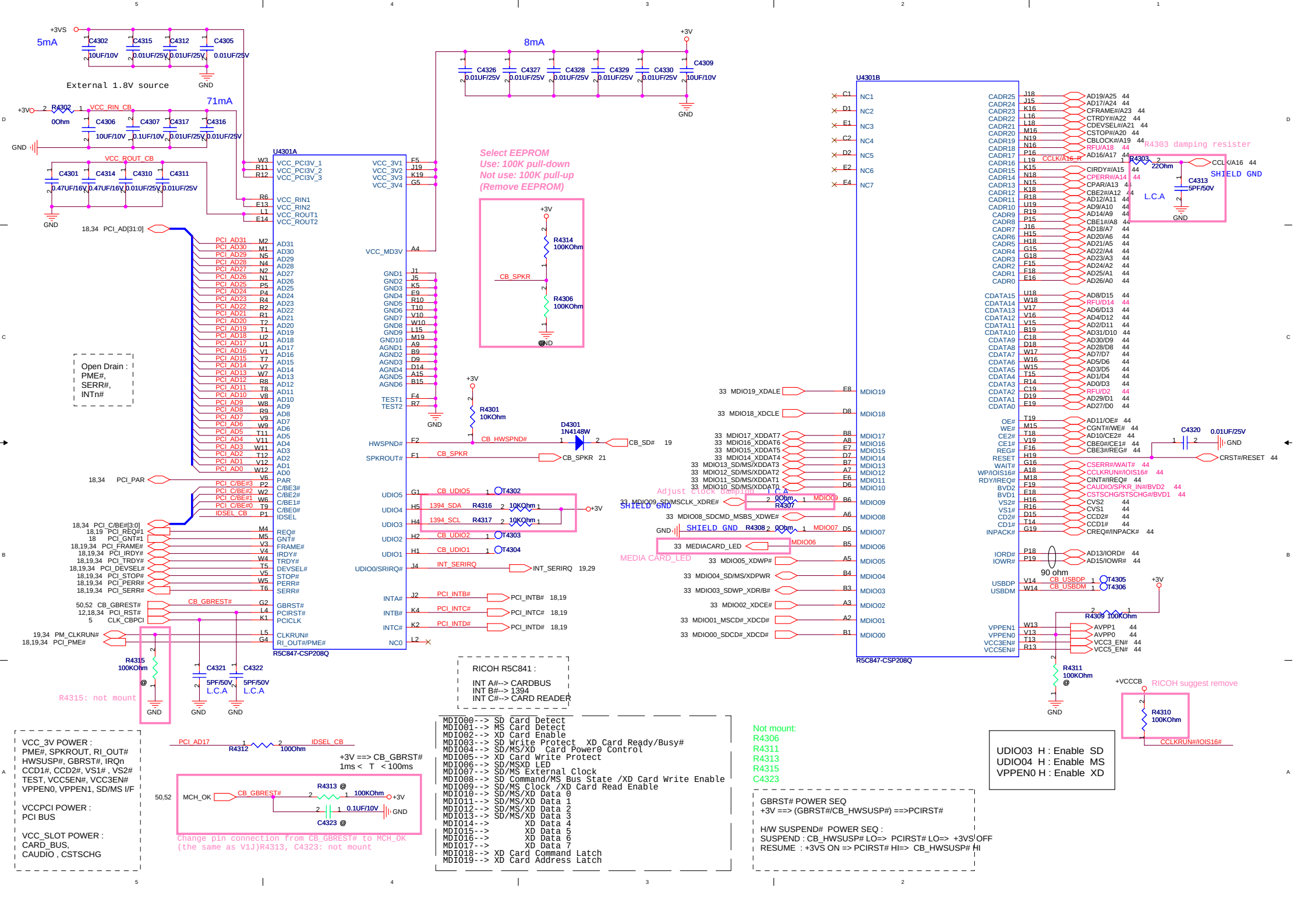


Without Battery & Pull out Adapter

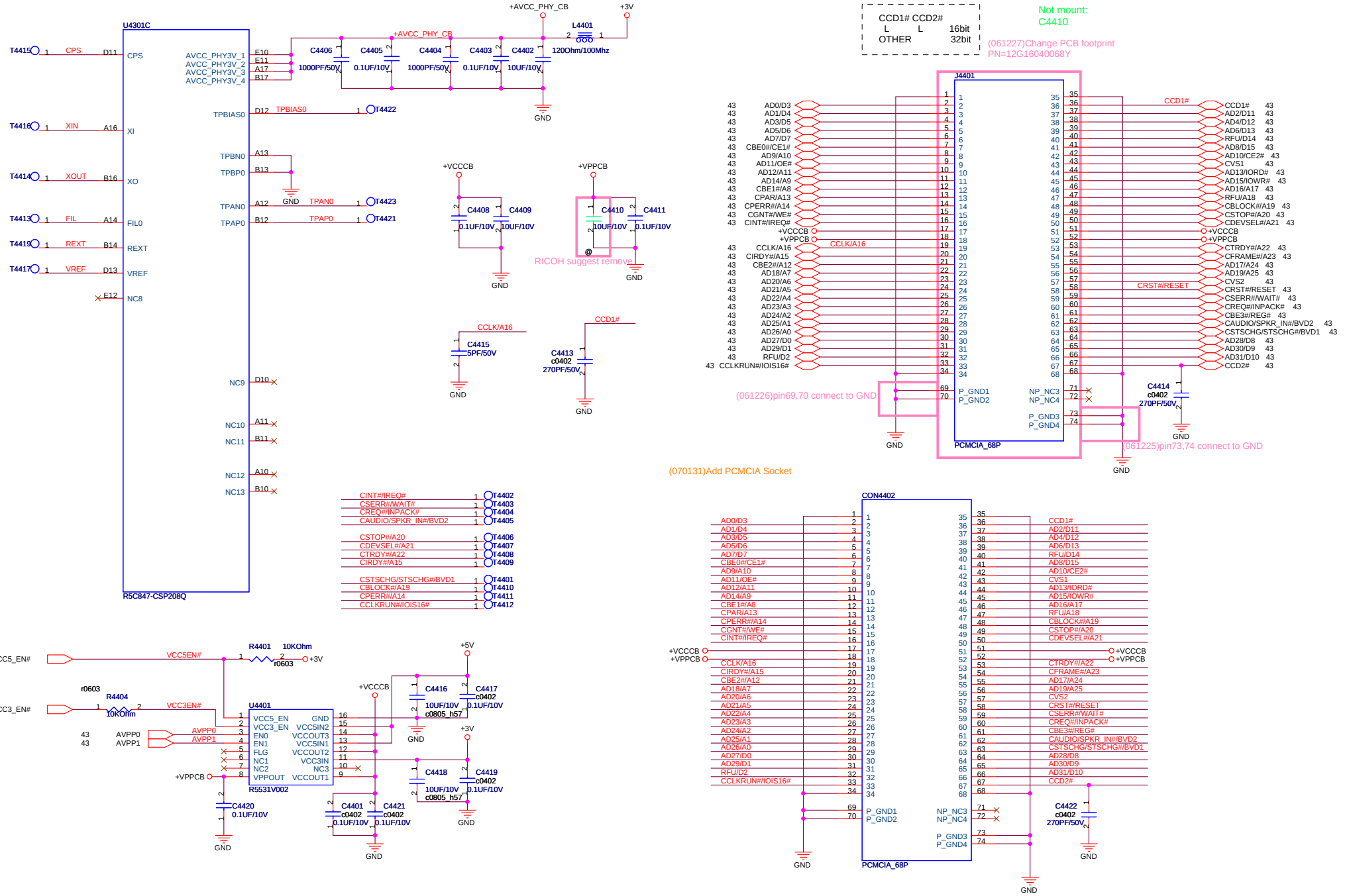







5mA
External 1.8V source
71mA
8mA
U4301A
R5C847-CSP208Q
U4301B
R5C847-CSP208Q
Select EEPROM
Use: 100K pull-down
Not use: 100K pull-up
(Remove EEPROM)
Open Drain : PME#, SERR#, INTn#
R4315: not mount
Change pin connection from CB_GBREST# to MCH_OK (the same as V1J)R4313, C4323: not mount
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
Not mount:
R4306
R4311
R4313
R4315
C4323
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
R4303 damping resister
SHIELD GND
L.C.A
90 ohm
RICOH suggest remove
+3V ==> CB_GBREST#
1ms < T < 100ms

PCMCIA SOCKET



CCD1# CCD2#
L L 16bit
OTHER 32bit

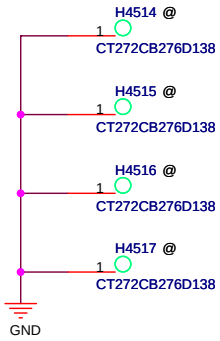
Not mount:
C4410

(061227)Change PCB footprint
PN=12G16040068Y

(070131)Add PCMCIA Socket

A:CPU BKT

PN:s01756



B:MDC NUT

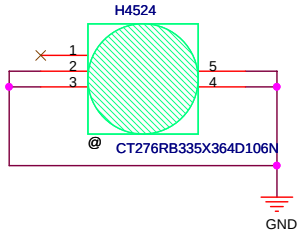
MDC NUT put on page35 (H3501, H3502)

F:MINI CARD NUT

MINI CARD NUT put on page26(H2601, H2602)

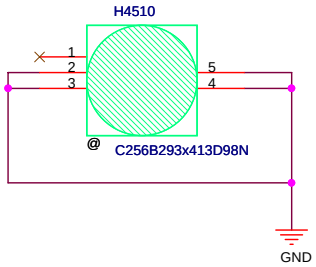
C:TOP TO BTM

PN:S01912



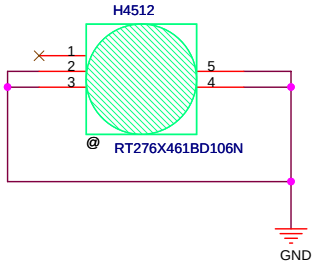
D:FIX MB

PN:s01769



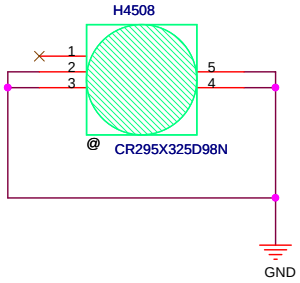
E:TOP TO BTM

PN:S01911



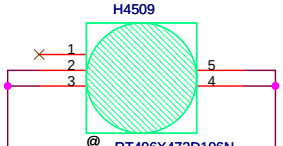
G:FIX MB

PN:s01783



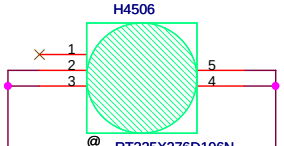
H:SYS BOSS

PN:S01914



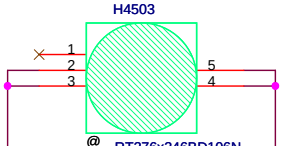
I:MB TO IO BKT

PN:S01913



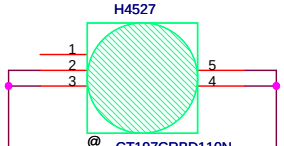
J:SYS BOSS

PN:S01915



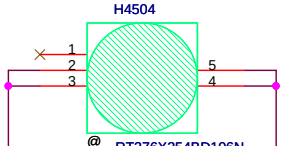
K:MB TO IO BKT

PN:S01705



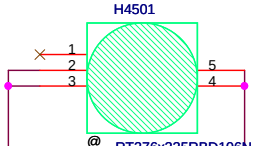
L:TOP TO BTM

PN:S01916



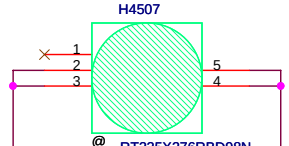
M:SYS BOSS

PN:s01917



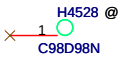
N:TOP TO BTM

PN:S01851



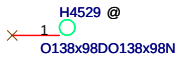
O:ALIGNMENT HOLE

PN:temp_5262_gh15



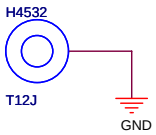
P:ALIGNMENT HOLE

PN:s01724



T:NB SINK NUT

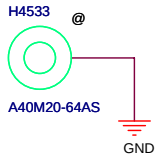
PN:13GNJ510M170-1



EMI NUT

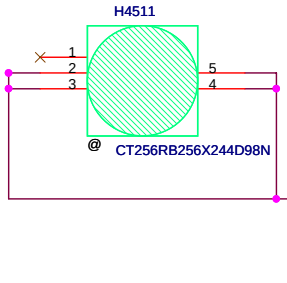
for LVDS cable

PN:13G021029050



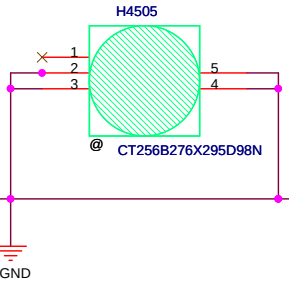
U:TOP TO BTM

PN:S01854



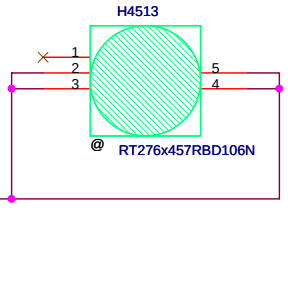
V:TOP TO BTM

PN:S01857



W:TOP TO BTM

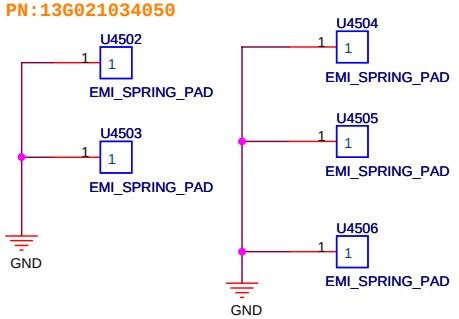
PN:S01918



GND

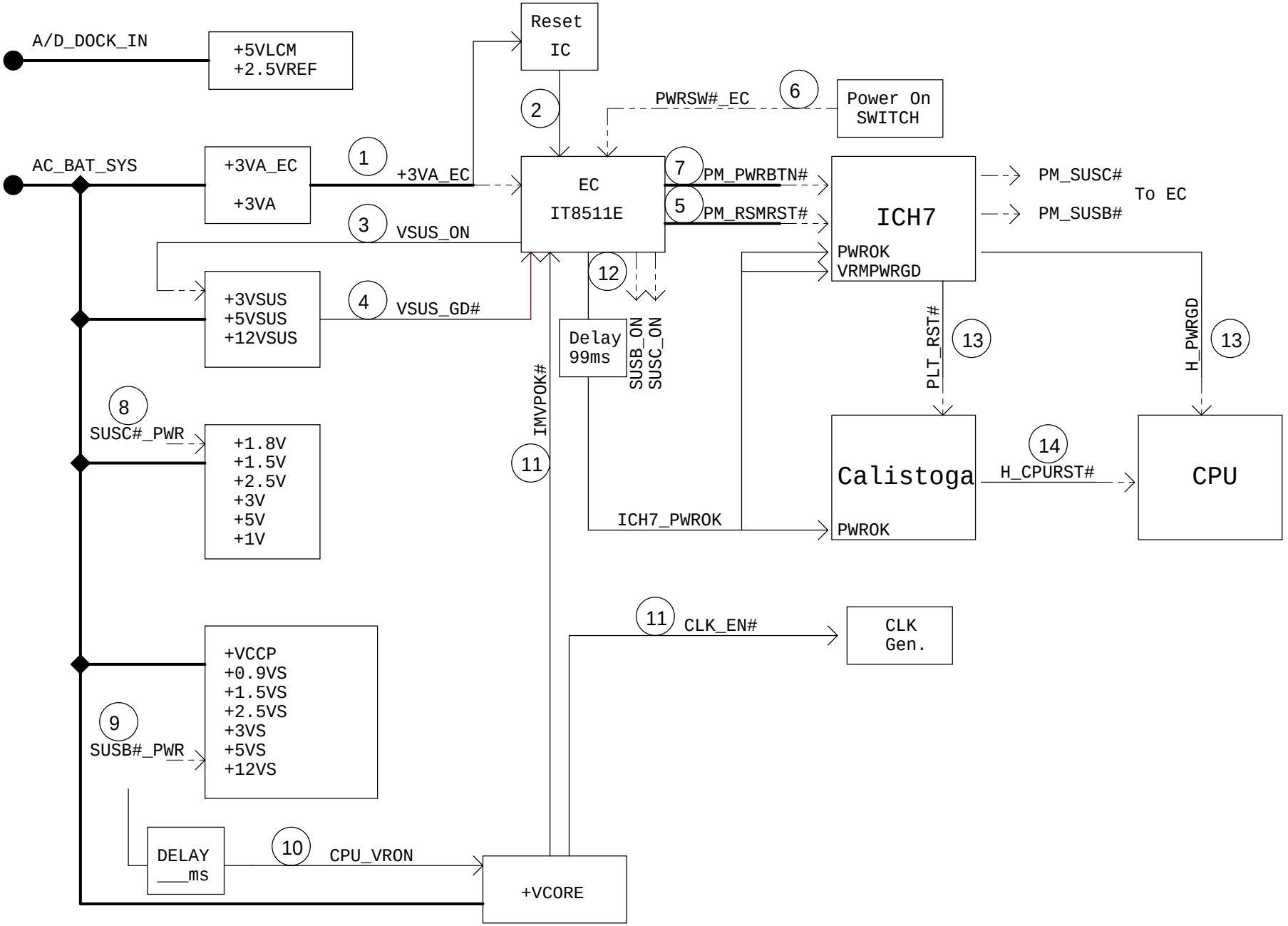
EMI SPRING

PN:13G021034050



R1.0 to R1.1

Page	Action
3	Change C304, C305, C306, C307, C308, C310, C312, C313 into 10UF for cost down.
4	Add R418 and Q404 to avoid error action.
7	Add R715 and R716 in other to improve signal quality.
12	Mount R1206 and Q1204 in other to reduce discharge time.
13	Change C1313, C1314 into 22PF in other to improve undershoot.
13	Change the rated current of the fuse(F1302) into 1A for customer's demand.
21	Mount R2105 and R2109, or there is no dialing tone.
21	Modify R2108 into 31.6Kohm in other to tune +5V_AUDIO.
21	Add three 0ohm resisters R2127, R2128, R2129 for EMI.
22	Change R2201~R2204 into 27Kohm for speaker volume.
22	Change 0ohm resisters(R2238, R2239) into beads.
22	Remove a N-MOS and a resistor on JACK_IN side due to change a new HP JACK.
22	Add 4 Varistors(D2202~D2205) for EMI.
23	Remove a N-MOS due to change a new MIC JACK.
23	Add a 120ohm bead L2304 and a 1000PF capacitor C2307 for EMI.
25	Add 0ohm resister R2503 and change Q2502 into unmount.
25	Add CON2502 in other to colayout with CON2501.
26	Connect not PCI_RST# but PLT_RST# to the RESET# signal of PCIE MiniCard for customer's demand.
27	Connect pin20 of MiniCard to the signal of OR conditions of WLAN_SW# and WLAN_ON# for customer's demand.
29	Change tolerance of R2918 into 1% and C2917 into 10% for the timing of EC_RST#.
29	Change WLAN_SW# into pull-up +3VSUS
30	Add 100PF capacitors C3011 and C3012 for EMI.
33	Add CON3302, RN3301, RN3302, RN3303, RN3304, RN3305 in other to colayout with CON3301.
33	Add Varistors D3304 and D3305 for EMI.
33	Change R3308 into 39ohm for the brightness of LED3301.
34	Change C3406, C3407 into 30PF in other to fit 25MHz frequency.
35	Place C3502, C3503 on the other side of L3503, L3504 for layout.
36	Change CE3602 from 100UF to 150UF in other to fit droop SPEC.
37	Change R3704, Q3705, R3708, Q3709, R3709, Q3710, R3710, Q3711, R3711, Q3711 into unmount because they don't affect the discharge circuit.
38	Change resisters R3805, R3806, R3807 into 620ohm in other to tune brightness.
41	Change the fuse F4101 into mount for customer's demand.
41	Add the colayout of JP4102 and F4102 for customer's demand.
41	Change 0ohm resister R4105 into 120ohm bead L4105 for EMI.
41	Add four Varistors D4102, D4103, D4104, D4105 and ten capacitors C4110~C4119 for EMI.
41	Chane C4103, C4104 into mount for EMI.
70	Chane R7002 into 80.6ohm for brightness.



Power ON Sequence

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/	O	55	GPH2	IMVPOK#	I
37	PWM3/GPA3	BAT_LOW_BEEP(Reserved)	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCHDOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/0	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/0	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RCIN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GPI7	/	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/0	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/0	101	DAC2/GPJ2	INVTER_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	/	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I			/	
1	CK32KOUT/GPC7	/	O			/	
26	RI1#/WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	BAT0_AD	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I	82	ADC1/GPK1	/	
30	LPCRST#/WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	AC_AD	I
31	ECSCI#/GPD3	ECSCI#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT/GPD5	/		94	ADC9/GPK5	KB_ID0	I
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	/	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/		106	GPL5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I	107	GPL6	/	
25	CLKRUN#/WUI7/GPE7	/	O	108	GPL7	/	
110	PS2CLK0/GPF0	/		22	ECSMI#/GPM0	EXTSMI#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#/GPM1	/	
114	PS2CLK1/GPF2	/	I/0	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/0	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	/	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	/	
118	PS2CLK3/GPF6	/					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

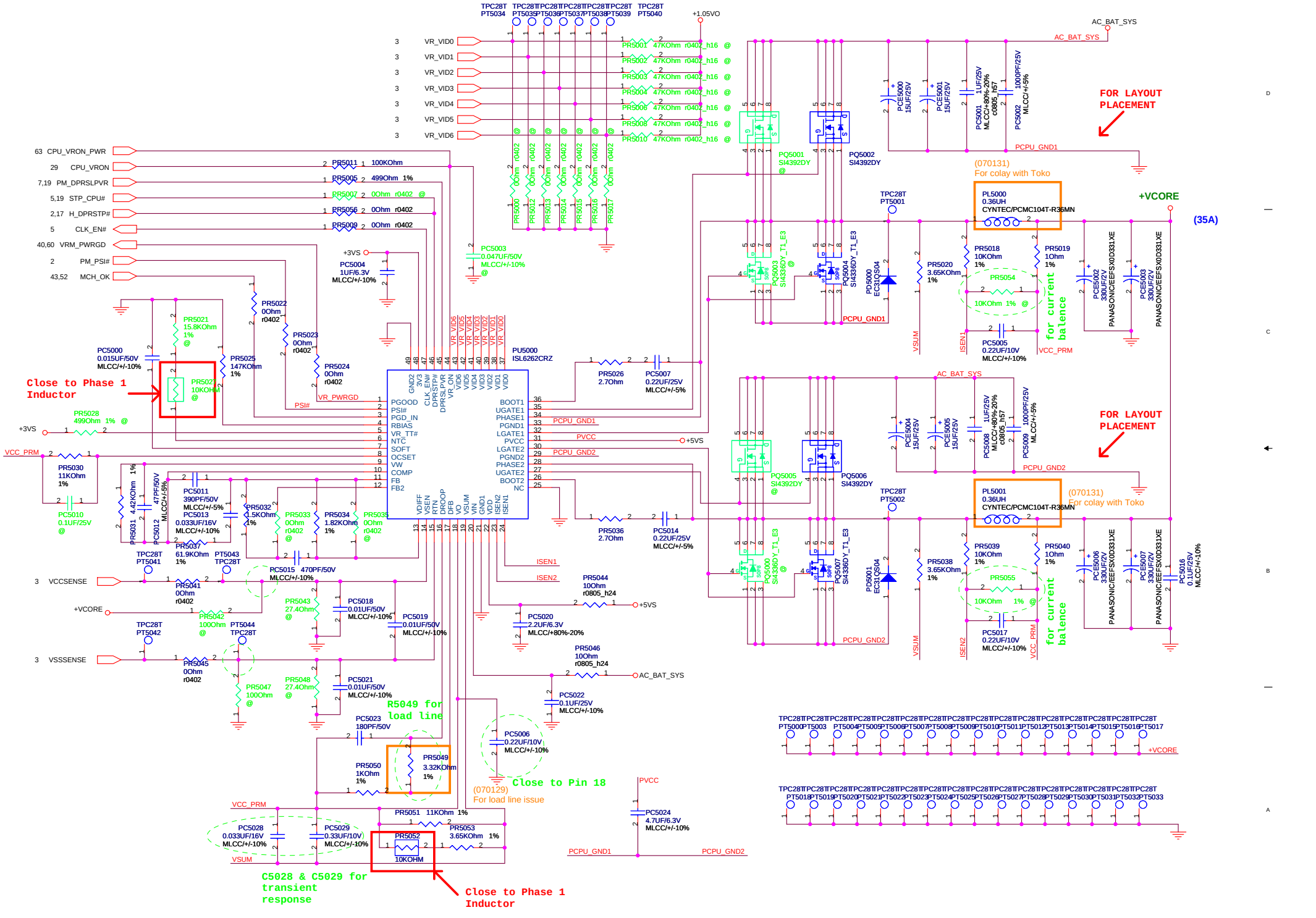
Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	/	I/O
AC18	GPIO07	PM_THERM#_GPIO (Reserved)	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_SW#_ICH	I
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	NEWCARD_DET#	I
R4	GPIO14	BAT_LL#_ICH (Reserved)	I
E22	GPIO15	WLAN_LED#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STPPCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STPCPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	REQ4#/GPIO22	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	CB_SD#	O
A21	GPIO26	/	
B21	GPIO27	BTO_DEV0	I
E23	GPIO28	NEWCARD_OFF#	O
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AC19	GPIO33/AZ_DOCK_EN#	BTO_DEV1	I
U2	GPIO34/AZ_DOCK_RST#	BTO_DEV2	I
AD21	GPIO35	/	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

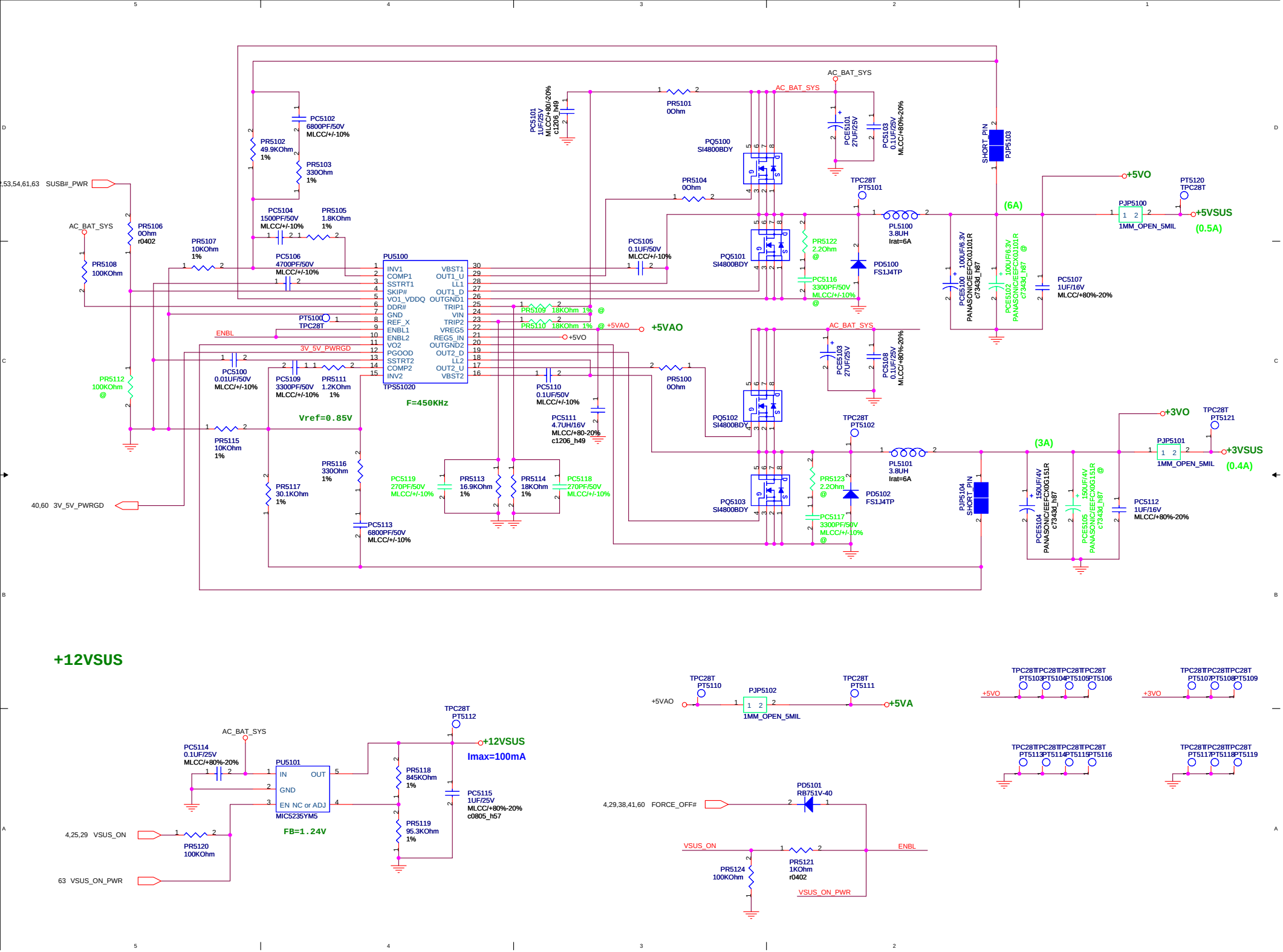
Indigo: the same as T12F
Pink: different from T12F

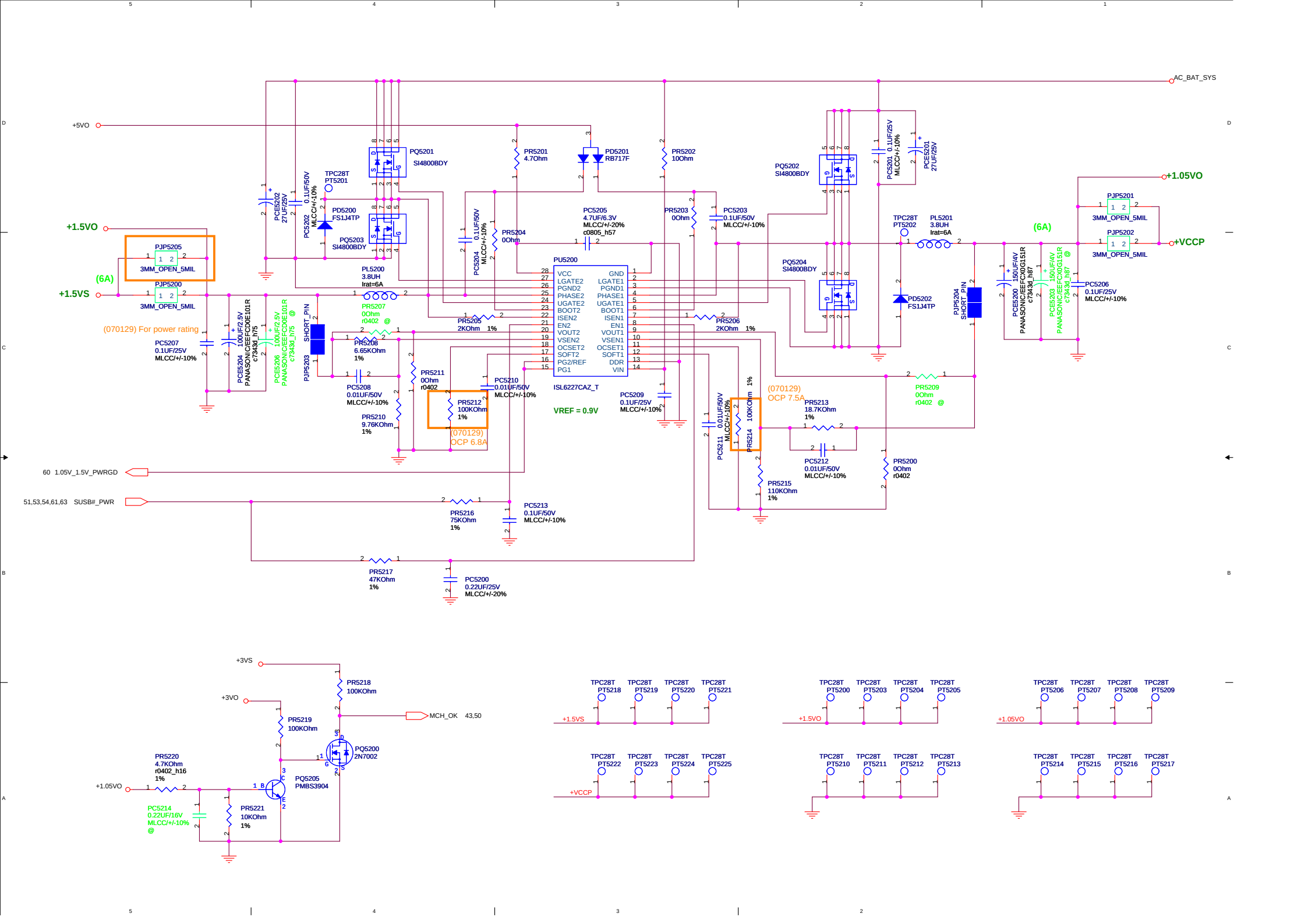
PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

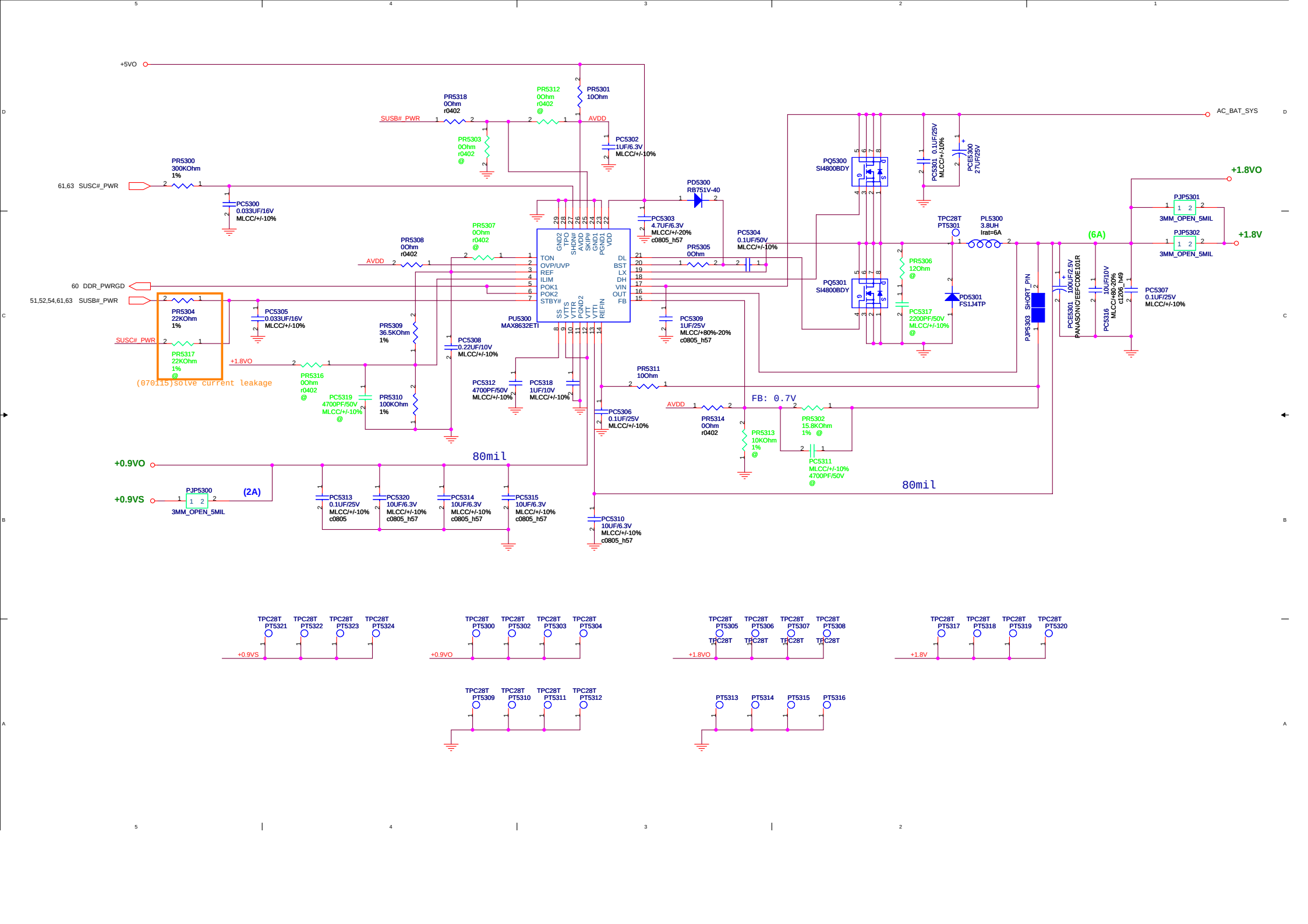
PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

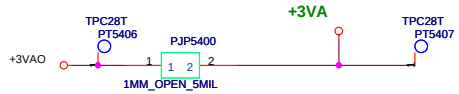

+1.05VO
AC_BAT_SYS
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
47KOhm r0402_h16
CPU_VRON_PWR
CPU_VRON
PM_DPRSLPVR
STP_CPU#
H_DPRSTP#
CLK_EN#
VRM_PWRGD
PM_PSI#
MCH_OK
100KOhm
499Ohm 1%
0Ohm r0402
+3VS
PU5000
ISL6262CRZ
PGOOD
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND1
VDD
ISEN2
ISEN1
PCPU_GND1
PCPU_GND2
+5VS
Close to Phase 1 Inductor
FOR LAYOUT PLACEMENT
(070131)
For colay with Toko
+VCORE
(35A)
PL5000
0.36UH
CYNTEC/PCMC104T-R36MN
PL5001
0.36UH
CYNTEC/PCMC104T-R36MN
PQ5001
PQ5002
PQ5005
PQ5006
SI4392DY
SI4336DY_T1_E3
PD5000
PD5001
EC31QS04
for current balence
VCC_PRM
VSUM
ISEN1
ISEN2
VCCSENSE
VSSSENSE
R5049 for load line
Close to Pin 18
(070129)
For load line issue
C5028 & C5029 for transient response
Close to Phase 1 Inductor

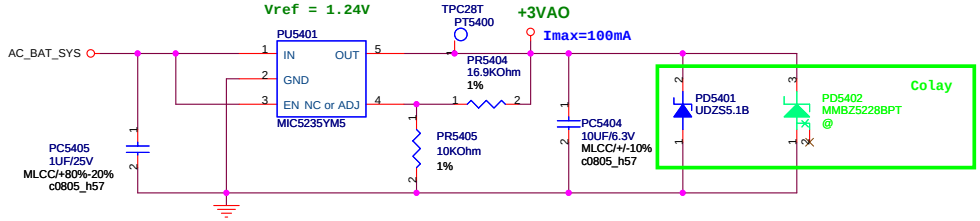

PU5100
TPS51020
F=450KHz
Vref=0.85V
PQ5100 SI4800BDY
PQ5101 SI4800BDY
PQ5102 SI4800BDY
PQ5103 SI4800BDY
PD5100 FS1J4TP
PD5102 FS1J4TP
PL5100 3.8UH Irat=6A
PL5101 3.8UH Irat=6A
PJP5100 1MM_OPEN_5MIL
PJP5101 1MM_OPEN_5MIL
PJP5102 1MM_OPEN_5MIL
PJP5103 SHORT_PIN
PJP5104 SHORT_PIN
+5VO
+5VAO
+5VSUS (0.5A)
+3VO
+3VSUS (0.4A)
(6A)
(3A)
AC_BAT_SYS
ENBL
3V_5V_PWRGD
40,60 3V_5V_PWRGD
53,54,61,63 SUSB#_PWR
+12VSUS
Imax=100mA
PU5101 MIC5235YM5
FB=1.24V
4,25,29 VSUS_ON
63 VSUS_ON_PWR
+5VA
4,29,38,41,60 FORCE_OFF#
PD5101 RB751V-40
VSUS_ON_PWR


AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
(6A)
PJP5205
3MM_OPEN_5MIL
PJP5200
3MM_OPEN_5MIL
(070129) For power rating
PC5207
0.1UF/25V
MLCC/+/-10%
PC5204
100UF/2.5V
PANASONIC/EEFCD0E101R
c7343d_h75
PC5206
100UF/2.5V
PANASONIC/EEFCD0E101R
c7343d_h75
SHORT_PIN
PJP5203
PQ5201
SI4800BDY
PQ5203
SI4800BDY
TPC28T
PT5201
PC5202
0.1UF/50V
MLCC/+/-10%
PC5202
27UF/25V
PD5200
FS1J4TP
PR5201
4.7Ohm
PD5201
RB717F
PR5202
10Ohm
PC5204
0.1UF/50V
MLCC/+/-10%
PR5204
0Ohm
PC5205
4.7UF/6.3V
MLCC/+/-20%
c0805_h57
PR5203
0Ohm
PC5203
0.1UF/50V
MLCC/+/-10%
PL5200
3.8UH
Irat=6A
PR5207
0Ohm
r0402 @
PR5205
2KOhm 1%
PR5206
2KOhm 1%
PR5208
6.65KOhm
1%
PR5211
0Ohm
r0402
PC5208
0.01UF/50V
MLCC/+/-10%
PR5210
9.76KOhm
1%
PR5212
100KOhm
1%
(070129)
OCP 6.8A
PC5210
0.01UF/50V
MLCC/+/-10%
PU5200
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
ISL6227CAZ_T
VREF = 0.9V
PC5209
0.1UF/25V
MLCC/+/-10%
PQ5202
SI4800BDY
PC5201
0.1UF/50V
MLCC/+/-10%
PCE5201
27UF/25V
PQ5204
SI4800BDY
TPC28T
PT5202
PL5201
3.8UH
Irat=6A
PD5202
FS1J4TP
PJP5204
SHORT_PIN
PR5209
0Ohm
r0402 @
(070129)
OCP 7.5A
PR5213
18.7KOhm
1%
PC5212
0.01UF/50V
MLCC/+/-10%
PR5214
100KOhm 1%
PC5211
0.01UF/50V
MLCC/+/-10%
PR5215
110KOhm
1%
PR5200
0Ohm
r0402
PCE5200
150UF/4V
PANASONIC/EEFCX0G151R
c7343d_h87
PCE5203
150UF/4V
PANASONIC/EEFCX0G151R
c7343d_h87 @
PC5206
0.1UF/25V
MLCC/+/-10%
PJP5201
3MM_OPEN_5MIL
PJP5202
3MM_OPEN_5MIL
+1.05VO
+VCCP
60 1.05V_1.5V_PWRGD
51,53,54,61,63 SUSB#_PWR
PR5216
75KOhm
1%
PC5213
0.1UF/50V
MLCC/+/-10%
PR5217
47KOhm
1%
PC5200
0.22UF/25V
MLCC/+/-20%
+3VS
+3VO
PR5218
100KOhm
MCH_OK 43,50
PR5219
100KOhm
PQ5200
2N7002
PR5220
4.7KOhm
r0402_h16
1%
+1.05VO
PQ5205
PMBS3904
PC5214
0.22UF/16V
MLCC/+/-10%
@
PR5221
10KOhm
1%
TPC28T PT5218 PT5219 PT5220 PT5221
+1.5VS
TPC28T PT5200 PT5203 PT5204 PT5205
+1.5VO
TPC28T PT5206 PT5207 PT5208 PT5209
+1.05VO
TPC28T PT5222 PT5223 PT5224 PT5225
+VCCP
TPC28T PT5210 PT5211 PT5212 PT5213
TPC28T PT5214 PT5215 PT5216 PT5217

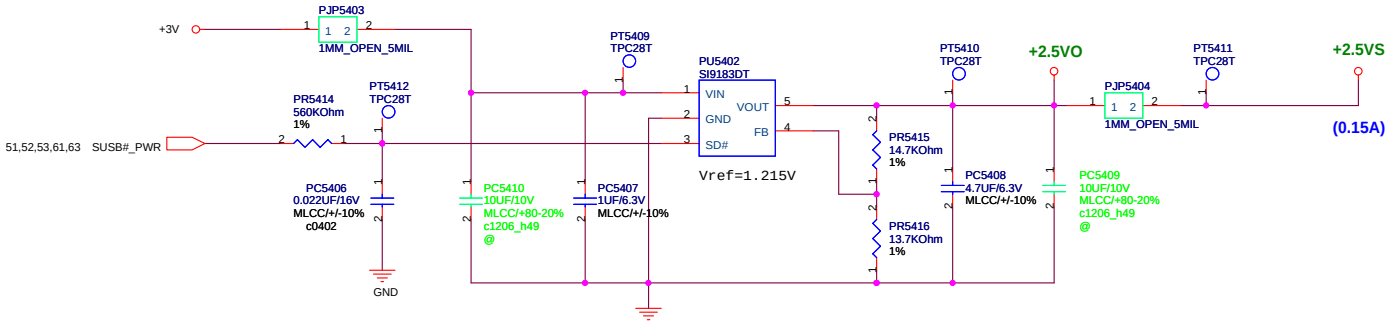

+5VO
PR5318 0Ohm r0402
SUSB# PWR
PR5312 0Ohm r0402 @
PR5301 10Ohm
AVDD
PR5303 0Ohm r0402 @
PC5302 1UF/6.3V MLCC/+/-10%
AC_BAT_SYS
PR5300 300KOhm 1%
61,63 SUSC#_PWR
PC5300 0.033UF/16V MLCC/+/-10%
PD5300 RB751V-40
PQ5300 SI4800BDY
PC5301 0.1UF/25V MLCC/+/-10%
PCE5300 27UF/25V
+1.8VO
PJP5301
3MM_OPEN_5MIL
PC5303 4.7UF/6.3V MLCC/+/-20% c0805_h57
PR5307 0Ohm r0402 @
PR5308 0Ohm r0402
PR5305 0Ohm
PC5304 0.1UF/50V MLCC/+/-10%
TPC28T PT5301
PL5300 3.8UH Irat=6A
(6A)
PJP5302
+1.8V
3MM_OPEN_5MIL
PQ5301 SI4800BDY
PR5306 12Ohm @
PD5301 FS1J4TP
PC5317 2200PF/50V MLCC/+/-10% @
60 DDR_PWRGD
51,52,54,61,63 SUSB#_PWR
PR5304 22KOhm 1%
PC5305 0.033UF/16V MLCC/+/-10%
SUSC# PWR
PR5317 22KOhm 1% @
(070115)solve current leakage
PU5300 MAX8632ETI
TON
OVP/UVP
REF
ILIM
POK1
POK2
STBY#
DL
BST
LX
DH
VIN
OUT
FB
GND2
TPO
SHDN#
AVDD
SKIP#
GND1
PGND1
VDD
SS
VTTS
VTTR
PGND2
VTTI
REFIN
PR5309 36.5KOhm 1%
PC5308 0.22UF/10V MLCC/+/-10%
PC5309 1UF/25V MLCC/+80%-20% c0805_h57
+1.8VO
PR5316 0Ohm r0402 @
PC5319 4700PF/50V MLCC/+/-10% @
PR5310 100KOhm 1%
PC5312 4700PF/50V MLCC/+/-10%
PC5318 1UF/10V MLCC/+/-10%
PR5311 10Ohm
PC5306 0.1UF/25V MLCC/+/-10%
AVDD
FB: 0.7V
PR5314 0Ohm r0402
PR5313 10KOhm 1% @
PR5302 15.8KOhm 1% @
PC5311 MLCC/+/-10% 4700PF/50V @
80mil
+0.9VO
+0.9VS
PJP5300
(2A)
3MM_OPEN_5MIL
PC5313 0.1UF/25V MLCC/+/-10% c0805
PC5320 10UF/6.3V MLCC/+/-10% c0805_h57
PC5314 10UF/6.3V MLCC/+/-10% c0805_h57
PC5315 10UF/6.3V MLCC/+/-10% c0805_h57
PC5310 10UF/6.3V MLCC/+/-10% c0805_h57
80mil
PJP5303 SHORT_PIN
PCE5301 100UF/2.5V PANASONIC/EEFCD0E101R
PC5316 10UF/10V MLCC/+80-20% c1206_h49
PC5307 0.1UF/25V MLCC/+/-10%
TPC28T PT5321
TPC28T PT5322
TPC28T PT5323
TPC28T PT5324
TPC28T PT5300
TPC28T PT5302
TPC28T PT5303
TPC28T PT5304
TPC28T PT5305
TPC28T PT5306
TPC28T PT5307
TPC28T PT5308
TPC28T PT5317
TPC28T PT5318
TPC28T PT5319
TPC28T PT5320
TPC28T PT5309
TPC28T PT5310
TPC28T PT5311
TPC28T PT5312
PT5313
PT5314
PT5315
PT5316

+3VAO

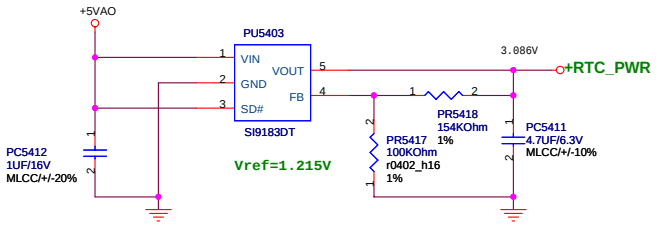




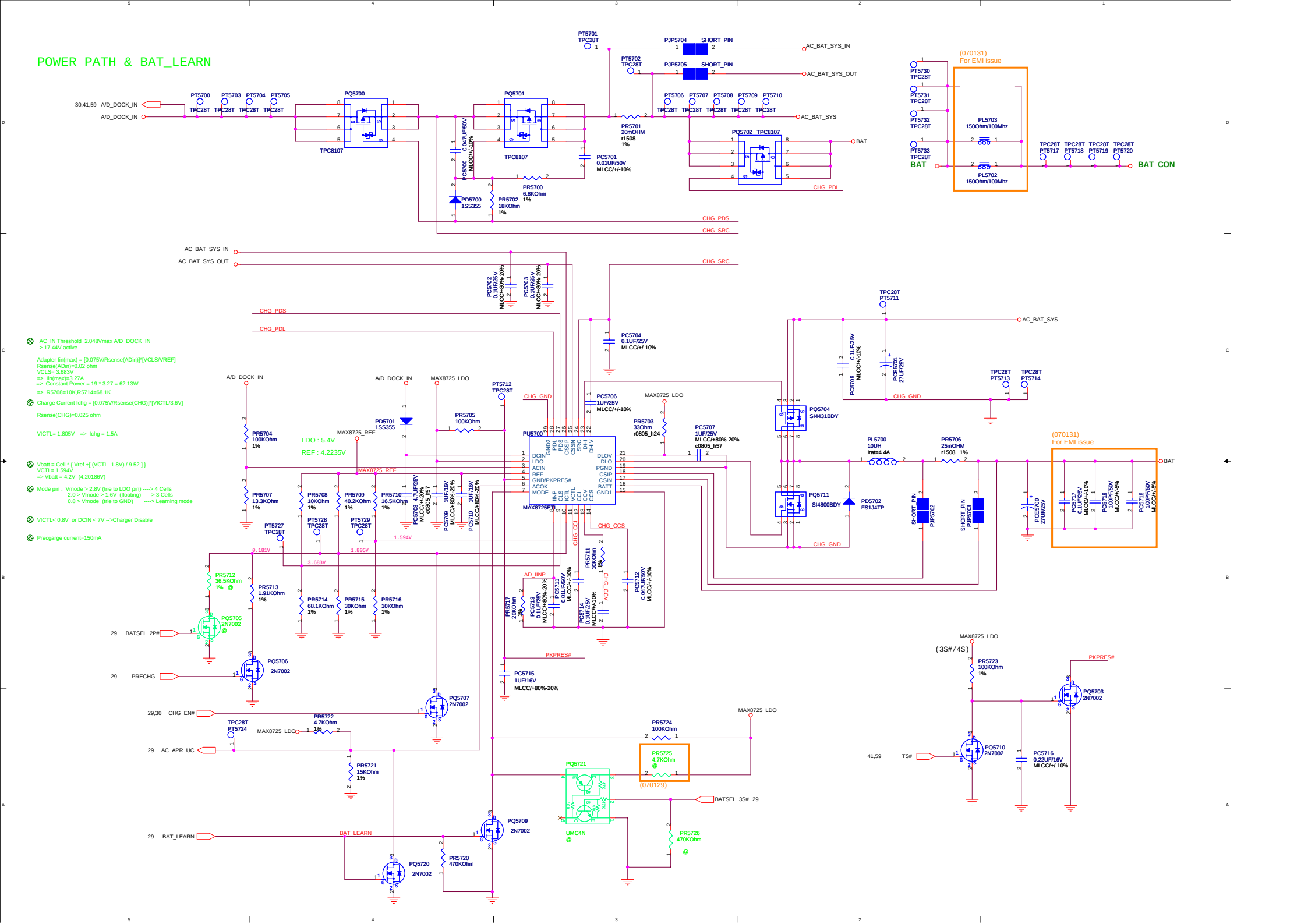
+2.5VS



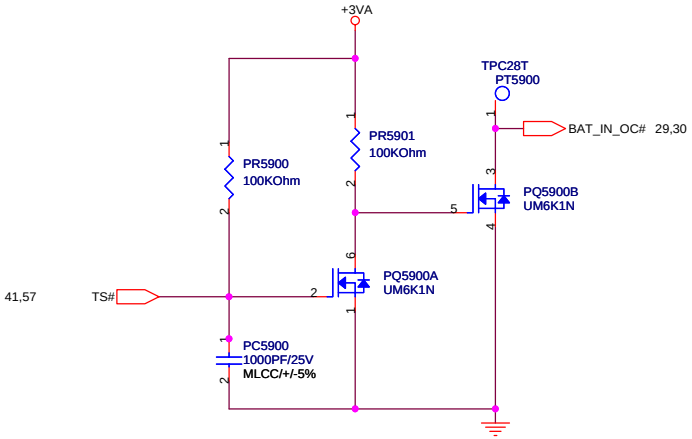
+RTC_PWR



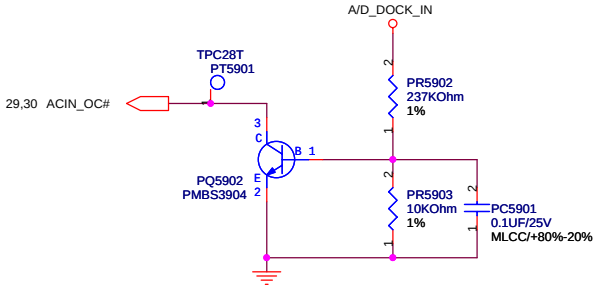
POWER PATH & BAT_LEARN



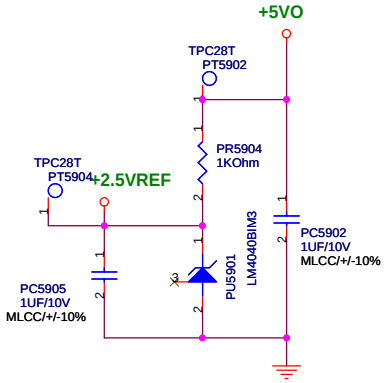
BATTERY IN DETECT



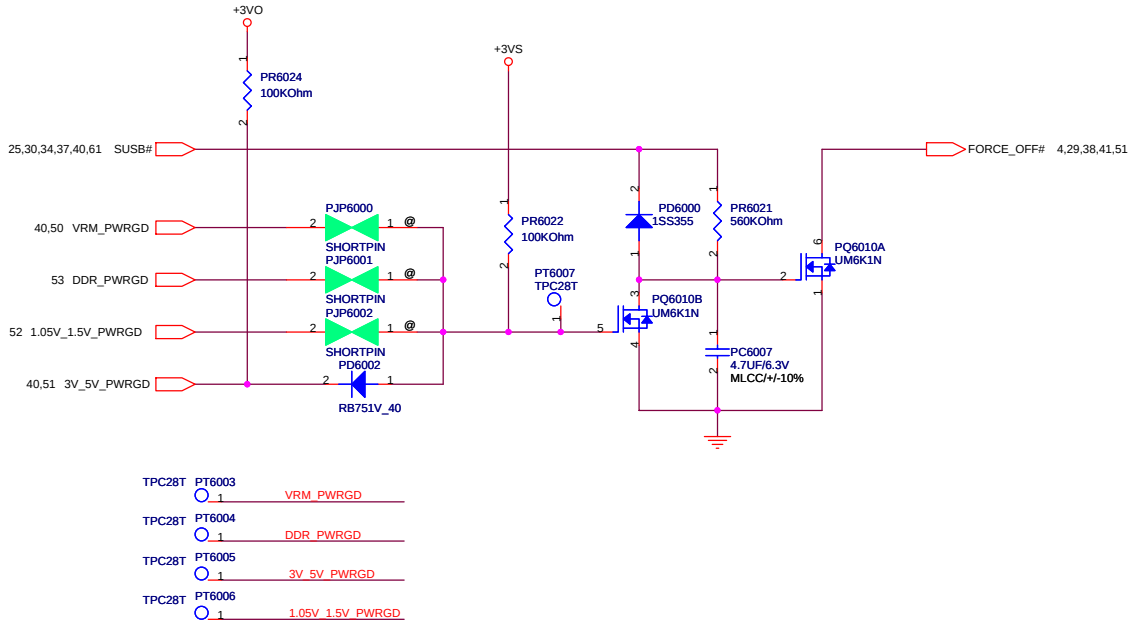
ADAPTER IN DETECT



+2.5VREF



POWER GOOD DETECTER



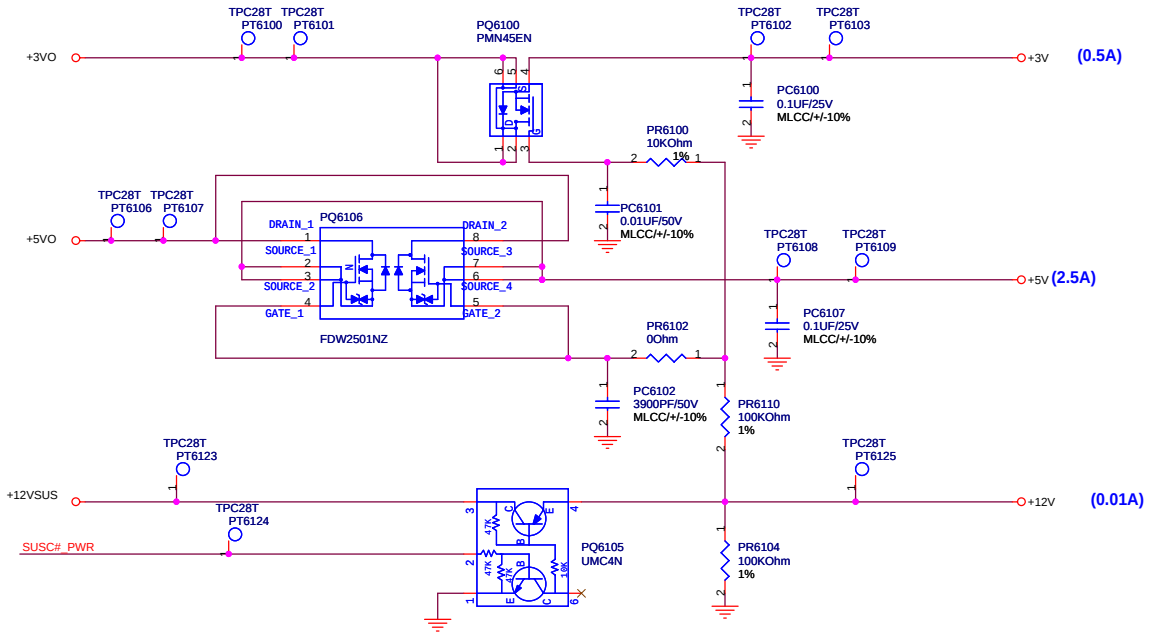
TPC28T PT6003 — VRM_PWRGD

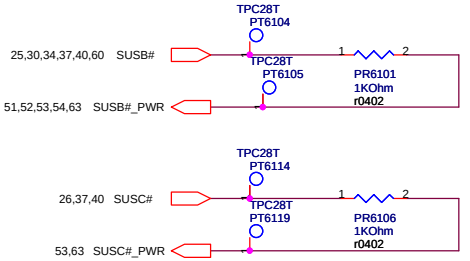
TPC28T PT6004 — DDR_PWRGD

TPC28T PT6005 — 3V_5V_PWRGD

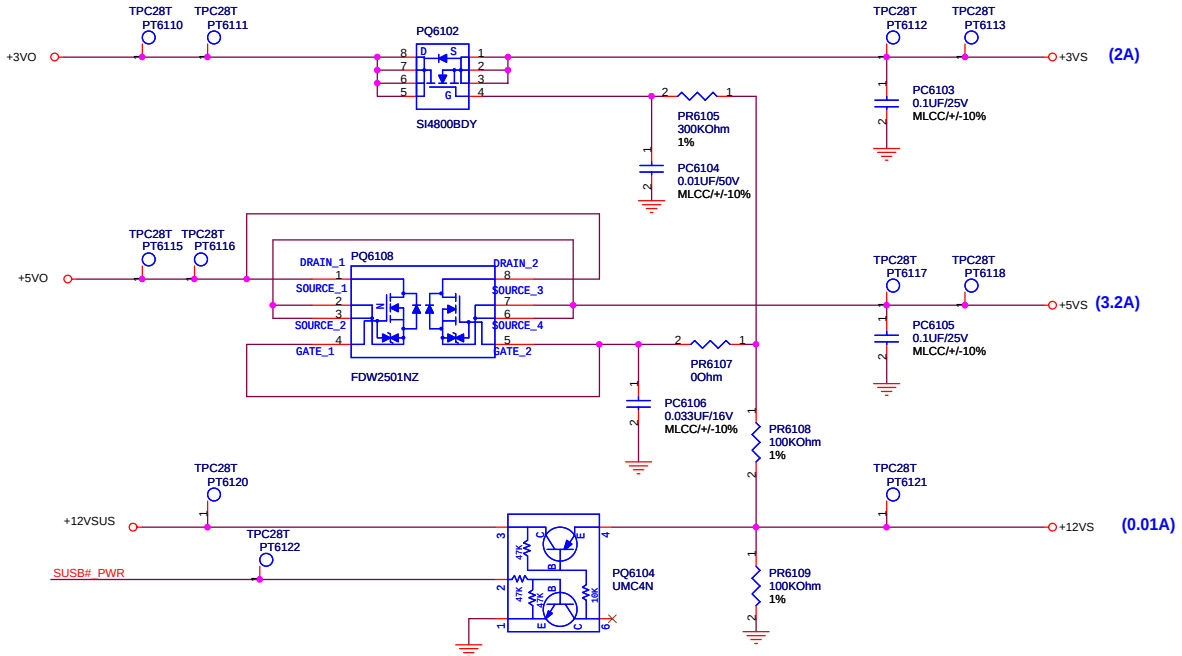
TPC28T PT6006 — 1.05V_1.5V_PWRGD

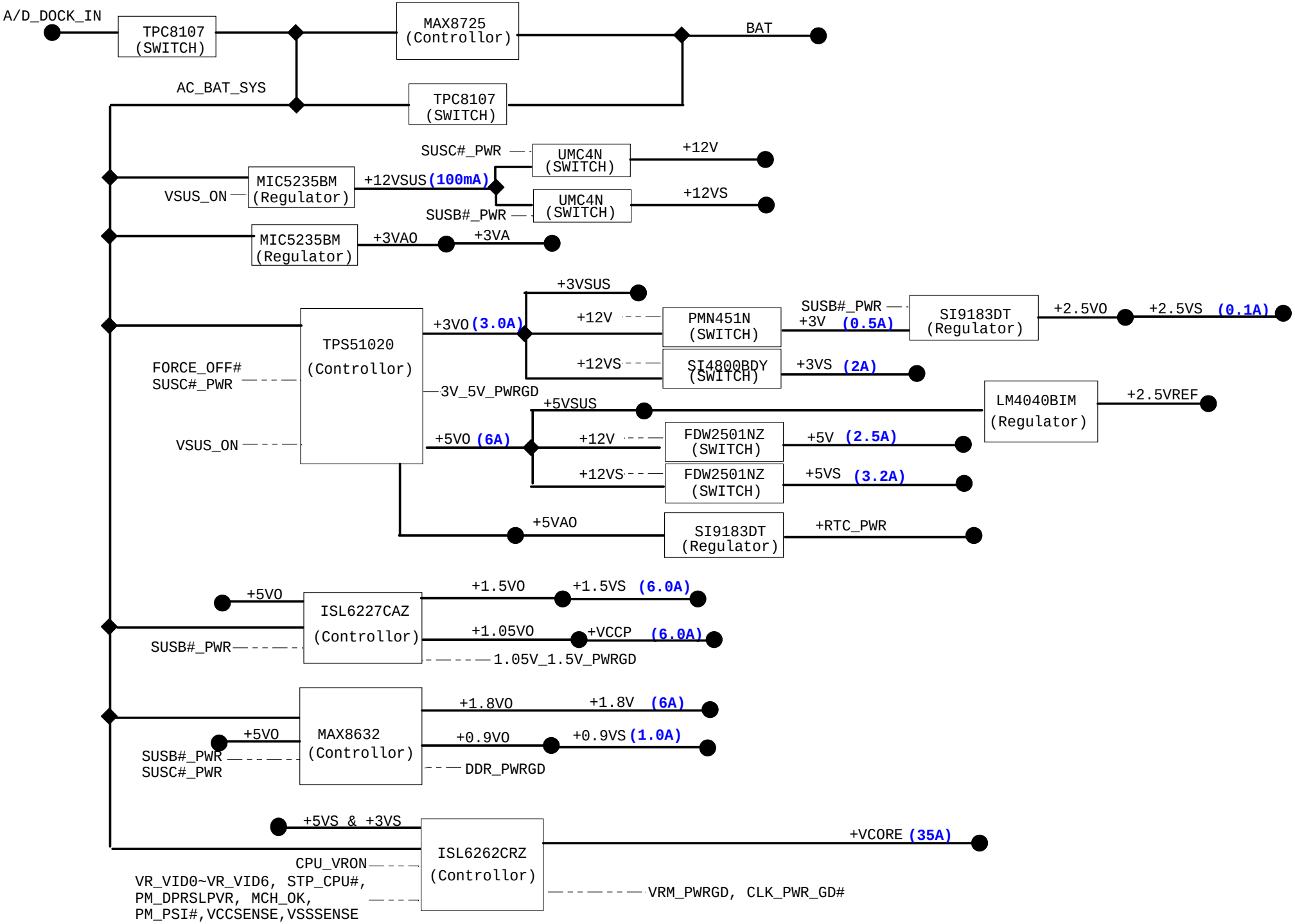
SUSC#_PWR POWER



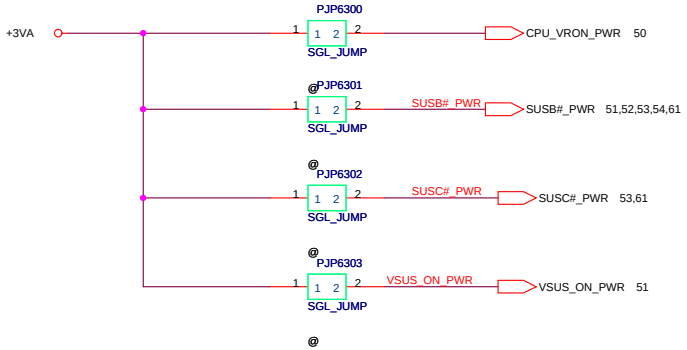


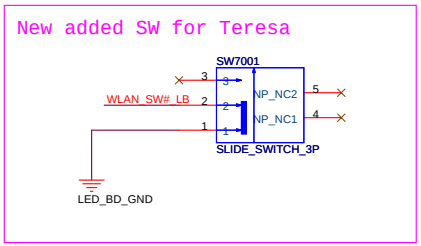
SUSB#_PWR POWER

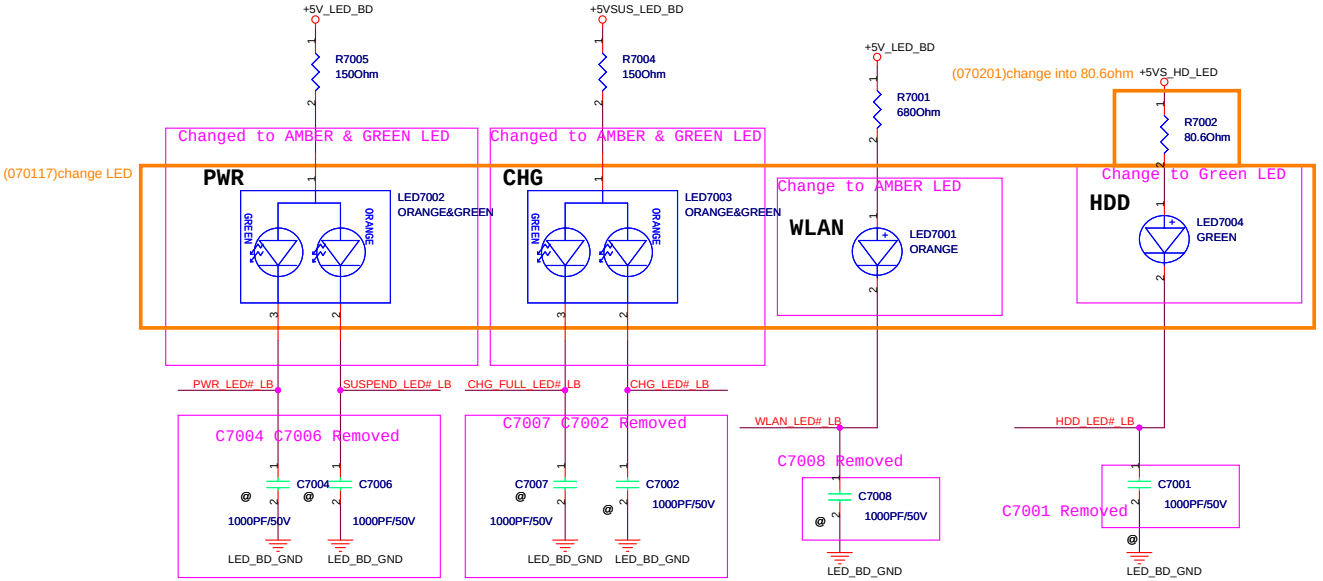


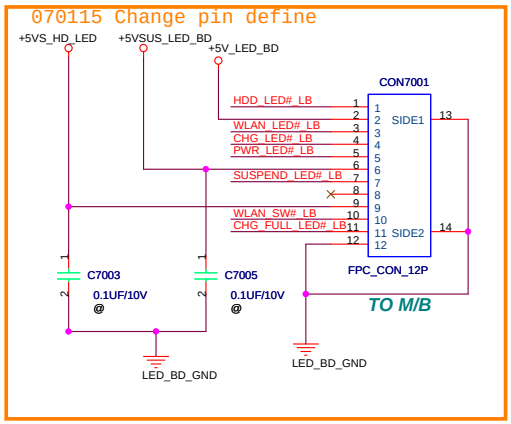

A/D_DOCK_IN
TPC8107 (SWITCH)
MAX8725 (Controllor)
BAT
AC_BAT_SYS
TPC8107 (SWITCH)
SUSC#_PWR
UMC4N (SWITCH)
+12V
MIC5235BM (Regulator)
VSUS_ON
+12VSUS (100mA)
UMC4N (SWITCH)
+12VS
SUSB#_PWR
MIC5235BM (Regulator)
+3VAO
+3VA
+3VSUS
TPS51020 (Controllor)
+3VO (3.0A)
+12V
PMN451N (SWITCH)
SUSB#_PWR
+3V (0.5A)
SI9183DT (Regulator)
+2.5VO
+2.5VS (0.1A)
FORCE_OFF#
SUSC#_PWR
+12VS
SI4800BDY (SWITCH)
+3VS (2A)
3V_5V_PWRGD
+5VSUS
LM4040BIM (Regulator)
+2.5VREF
VSUS_ON
+5VO (6A)
+12V
FDW2501NZ (SWITCH)
+5V (2.5A)
+12VS
FDW2501NZ (SWITCH)
+5VS (3.2A)
+5VAO
SI9183DT (Regulator)
+RTC_PWR
+5VO
ISL6227CAZ (Controllor)
+1.5VO
+1.5VS (6.0A)
+1.05VO
+VCCP (6.0A)
SUSB#_PWR
1.05V_1.5V_PWRGD
+1.8VO
+1.8V (6A)
MAX8632 (Controllor)
+5VO
+0.9VO
+0.9VS (1.0A)
SUSB#_PWR
SUSC#_PWR
DDR_PWRGD
+5VS & +3VS
ISL6262CRZ (Controllor)
+VCORE (35A)
CPU_VRON
VR_VID0~VR_VID6, STP_CPU#,
PM_DPRSLPVR, MCH_OK,
PM_PSI#,VCCSENSE,VSSSENSE
VRM_PWRGD, CLK_PWR_GD#

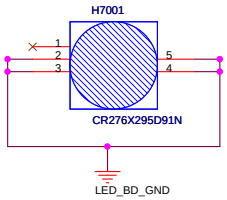
FOR POWER TEST



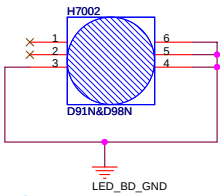








DETAIL: Q



DETAIL: S

Toshiba Satellite L40 schematic rev 1.1